



# A880GM-M6

Rev:1.0

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## REVISION HISTORY:

Rev	Date	Notes
A	2008-11-04	INITIAL RELEASE
1.0	2009-03-11	1. Change CPU Side Band Interface Connection. 2. Change CLK IC to ICS9LPRS471CS. 3. Modify CPU Vcore PWROK input level. 4. Change VCC_SB's GPIO Control Pin. 5. Modify HDMI/DVI switch and Hot-plug detection circuit. 6. Remove U10 which for the JMB362 1.8V, Direct Connect to VCC1.8. 7. Change Audio output Capacitance. 8. Change ATX12V 4 Pin to 8 Pin.
1.0	2009-06-08	1. Change the Model name to A785GM-M. 2. Add R33 for Plug only HDMI / DVI will be leakage to VCC3. 3. Change the PI3HDMI412FT-BZHES to ASM1445:(02-342-445070), Because of Leakage from the PI3HDMI412FT output differential line.
1.1	2009-09-24	Add NB_rst to LDT_RST for ACC.
1.0	2010-04-19	Change the title to A880GM-M6 V1.0.

### IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

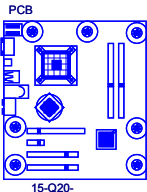
1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.



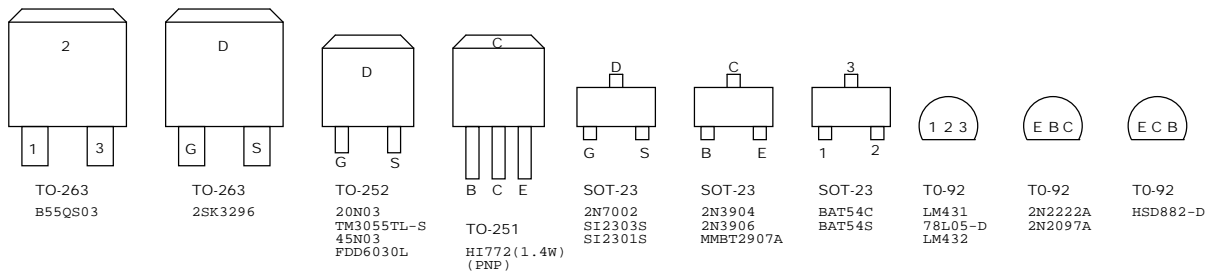
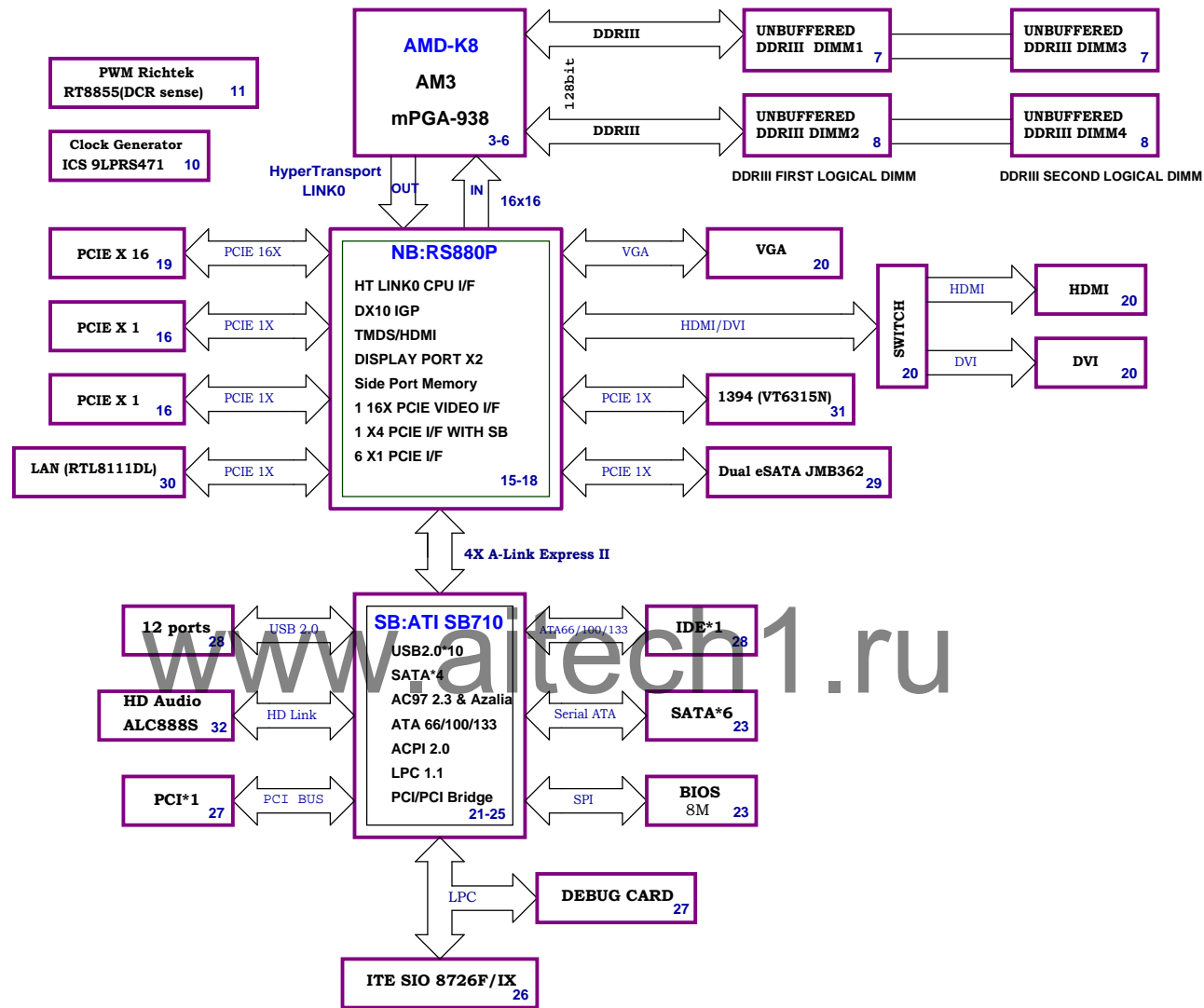
3) DESIGN NOTES in red are critical, and must be understood and followed.



PCB STACK: L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM

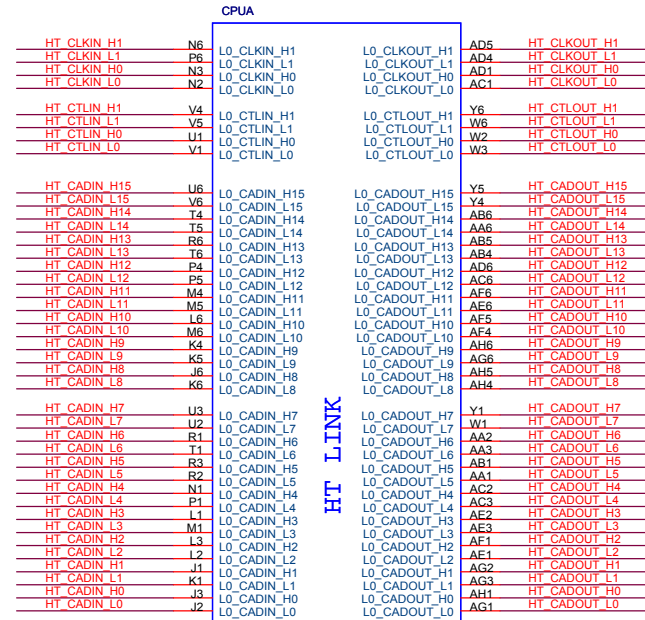
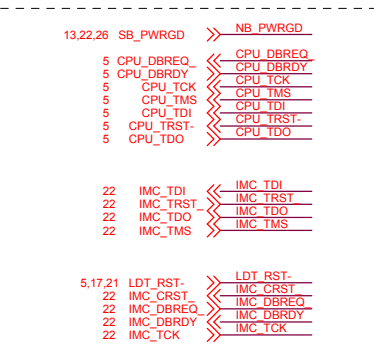
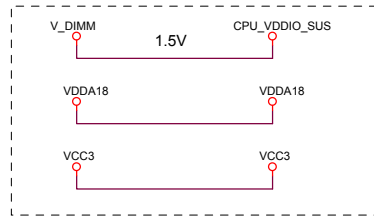
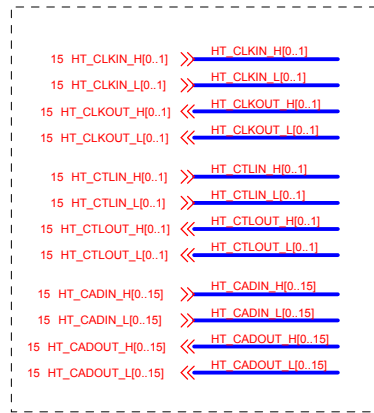
Elitegroup Computer Systems			
Title			
Cover Page			
Size	Document Number	Rev	
Custom	A880GM-M6	1.0	
Date:	Thursday, April 29, 2010	Sheet	1 of 36



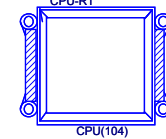
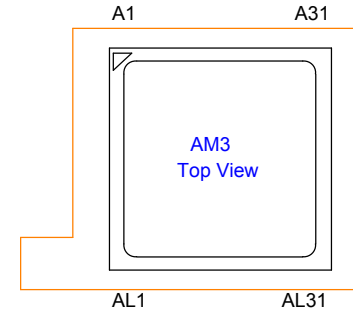




# HyperTransport

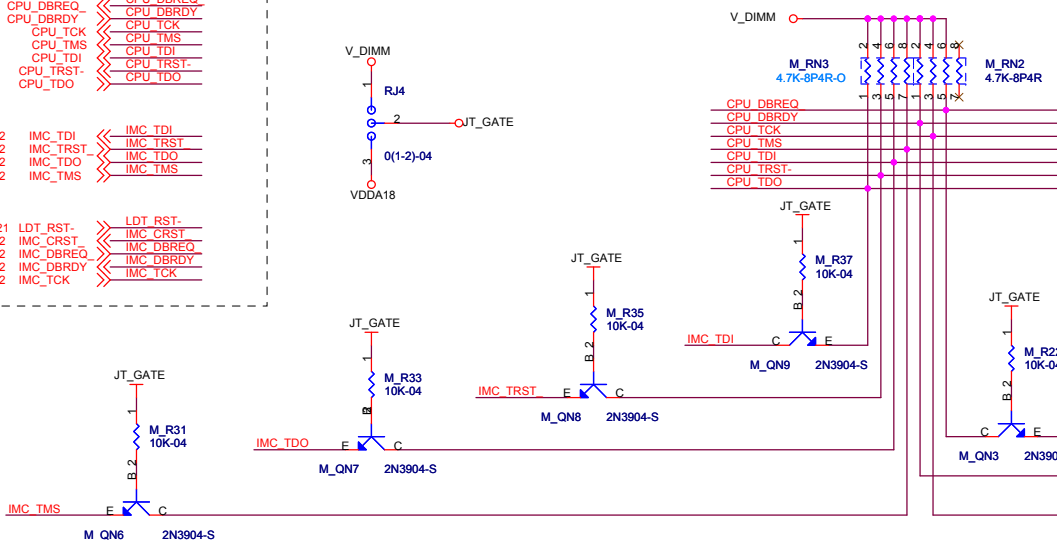
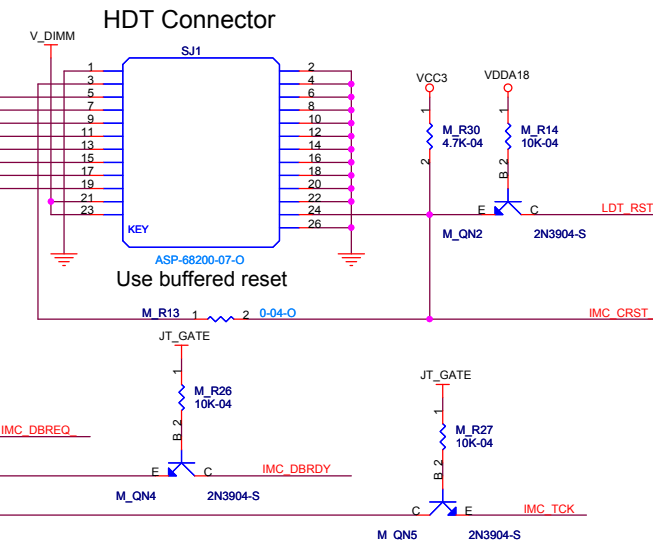
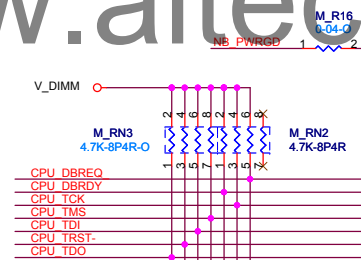


Please use 1mm pad size,  
place all ELT test pads  
on bottom side only.



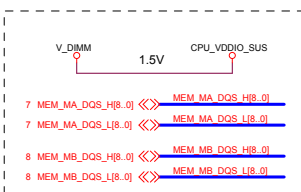
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Over Clocking

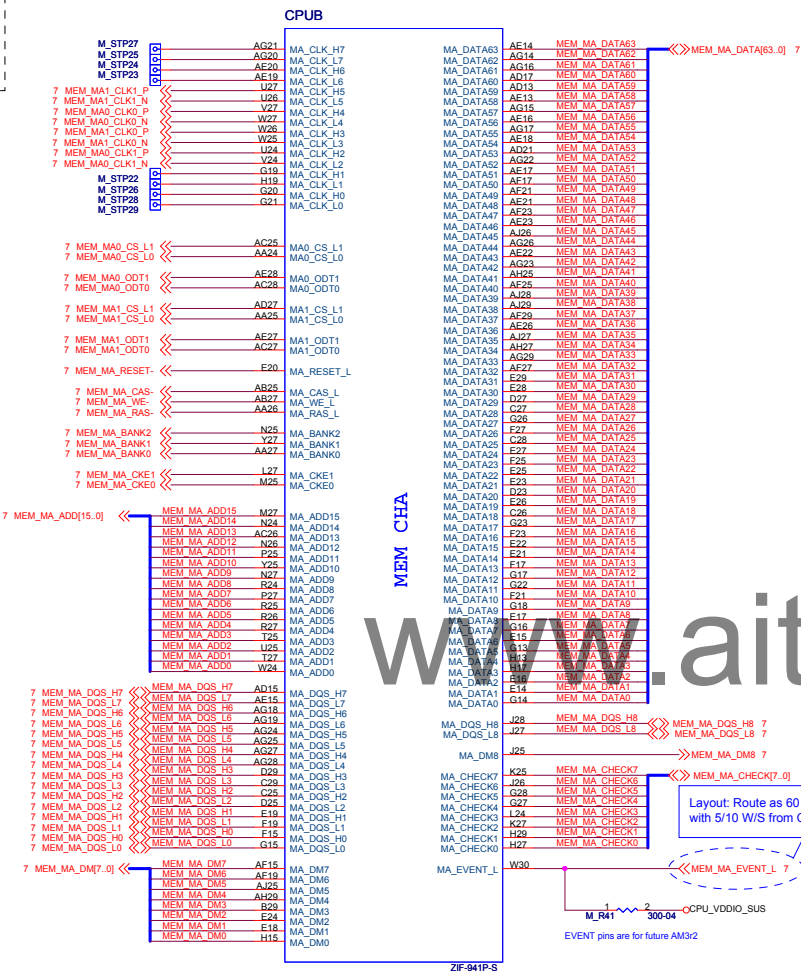




# CPU Memory



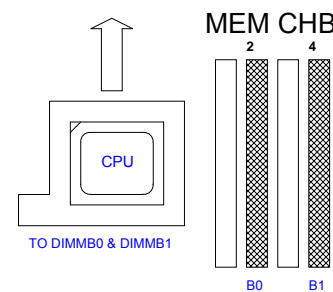
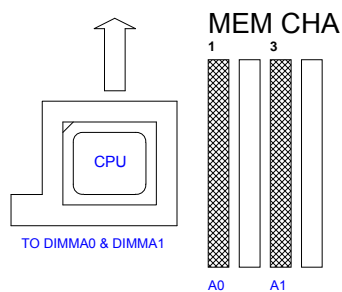
## DDR3 Memory Interface A



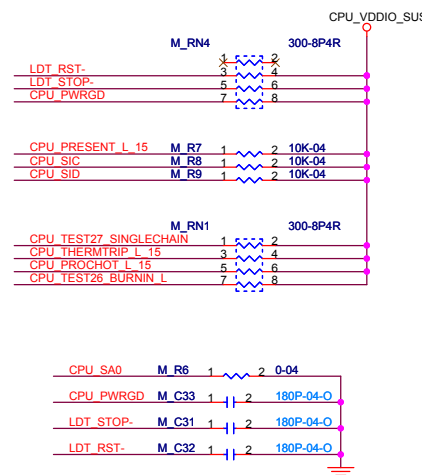
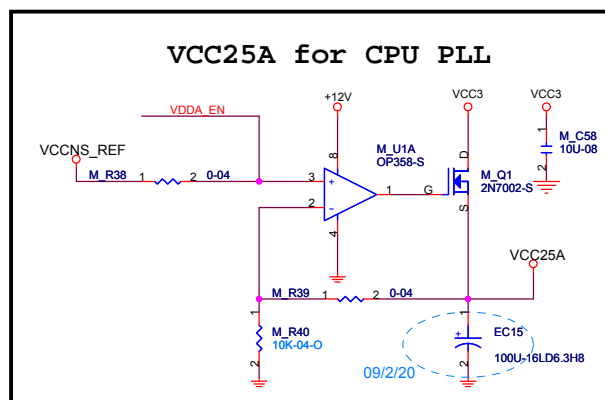
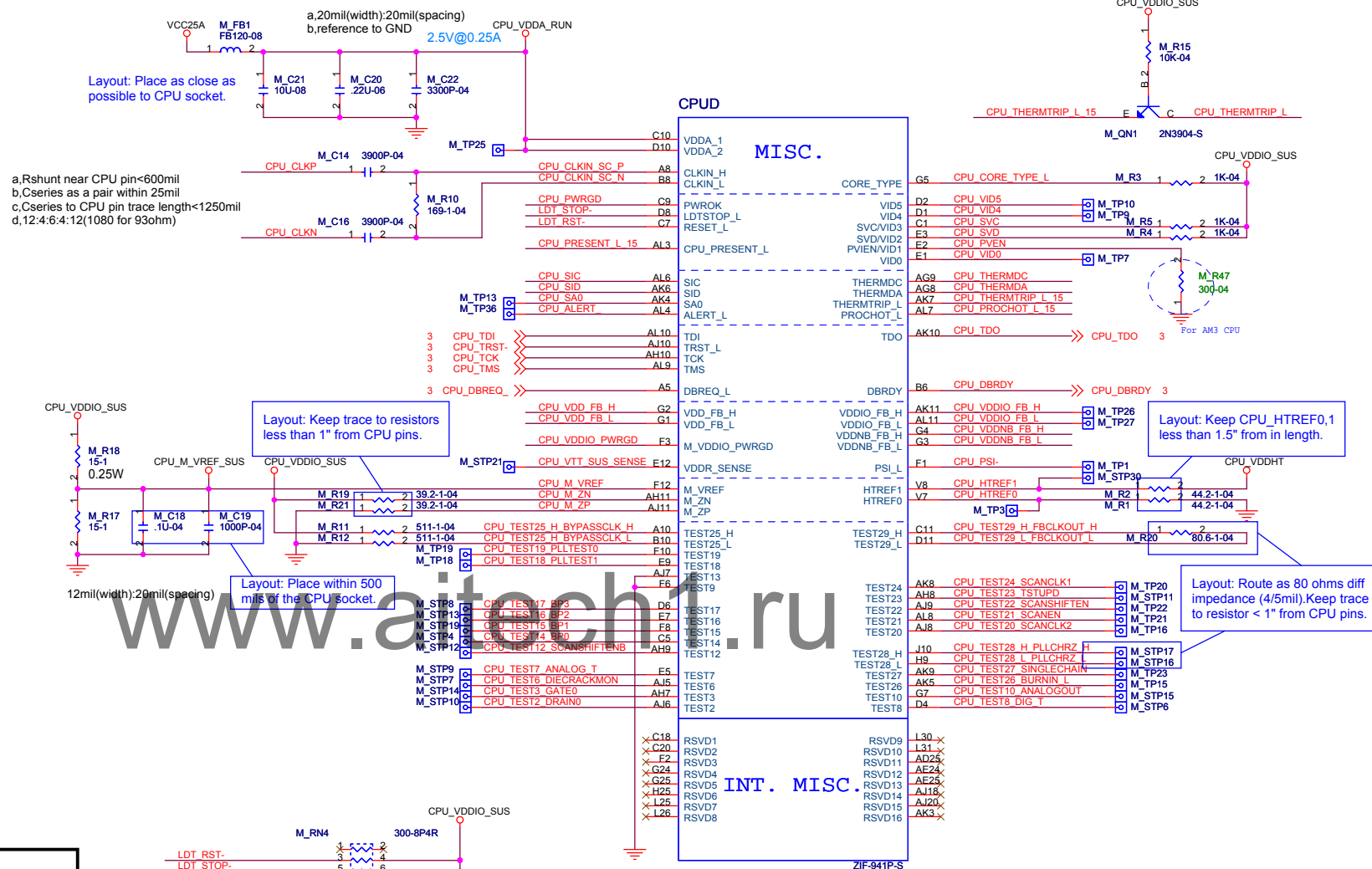
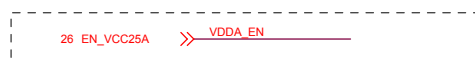
## DDR3 Memory Interface B



MEMORY CLOCK TRANSLATION		
DIMM	DDR2 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK1	MA_CLK2
	MEM_MA0_CLK0	MA_CLK4
DIMM A1	MEM_MA1_CLK1	MA_CLK5
	MEM_MA1_CLK0	MA_CLK3
DIMM B0	MEM_MB0_CLK1	MB_CLK2
	MEM_MB0_CLK0	MB_CLK4
DIMM B1	MEM_MB1_CLK1	MB_CLK5
	MEM_MB1_CLK0	MB_CLK3



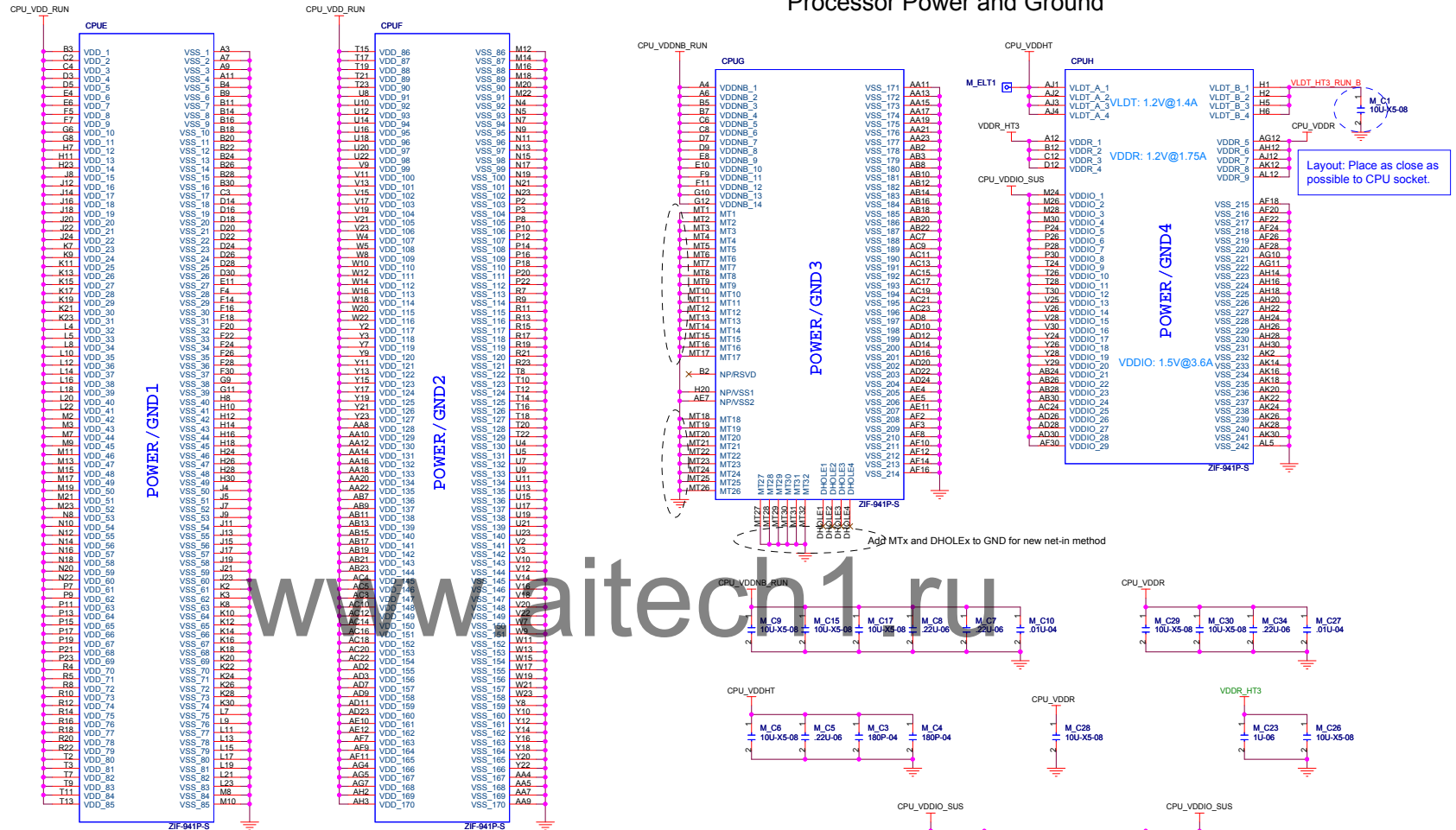




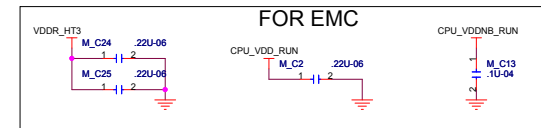


Timing diagram showing voltage levels for various components:

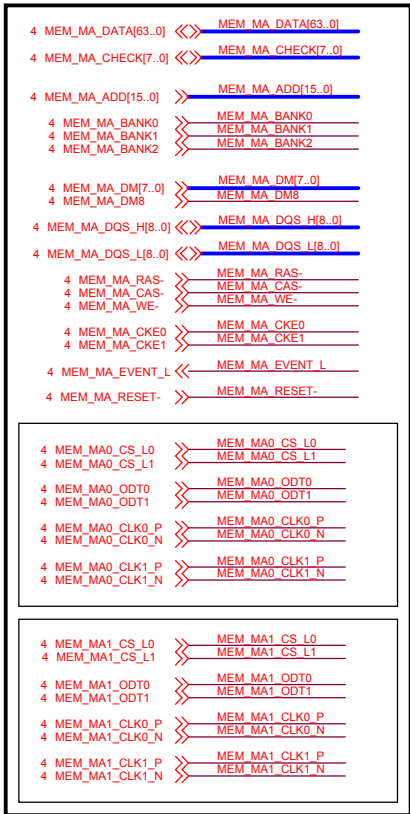
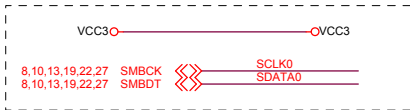
- VDDHT (1.2V) and CPU\_VDDHT (1.2V)
- VDDNB (1.5V) and CPU\_VDDNB (1.5V)
- VDIMM (1.5V) and CPU\_VDDIO\_SUS (1.5V)
- VDDCORE (1.5V) and CPU\_VDDCORE\_RUN (1.5V)



The image displays a detailed PCB layout for a power management section. It features four main power planes: CPU\_VDDIO\_SUS, CPU\_VDDIO\_RUN, CPU\_VDDNB\_RUN, and CPU\_VDD\_RUN. Each plane is populated with numerous decoupling capacitors, labeled with identifiers such as M\_SC37, M\_SC36, M\_SC32, M\_SC34, M\_SC33, M\_SC28, M\_SC31, M\_SC30, M\_SC35, M\_SC29, M\_C11, M\_C12, M\_SC8, M\_SC13, M\_SC19, M\_SC4, M\_SC22, M\_SC15, M\_SC21, M\_SC24, M\_SC23, M\_SC20, M\_SC11, M\_SC17, M\_SC2, M\_SC1, M\_SC5, M\_SC14, M\_SC10, M\_SC9, M\_SC18, M\_SC12, M\_SC25, M\_SC26, M\_SC27, M\_SC16, M\_SC3, M\_SC7, and M\_SC6. The capacitors are connected to various voltage rails, including 220uF, 100uF, 10uF, and 180pF. The layout also shows a network of interconnecting traces and vias, ensuring proper power distribution and signal integrity across the board.

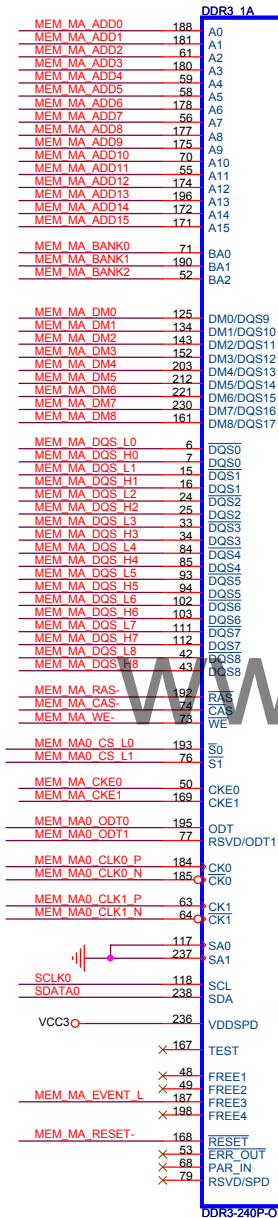




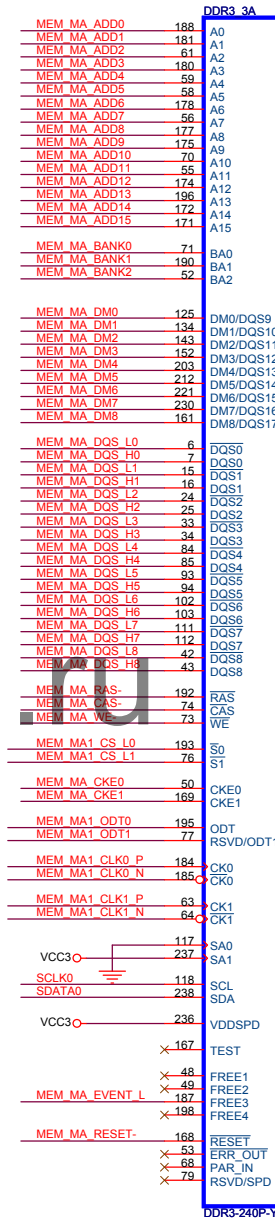


## SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

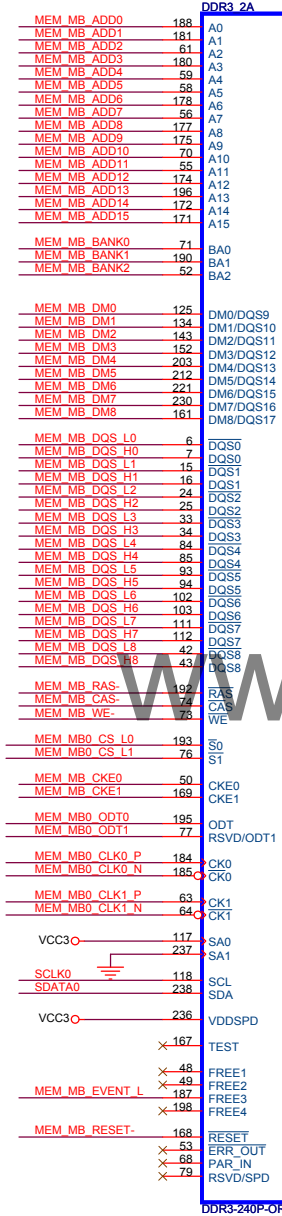
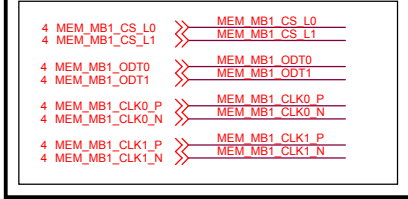
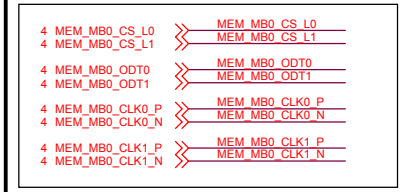
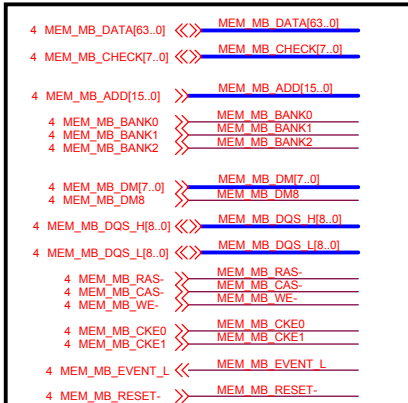
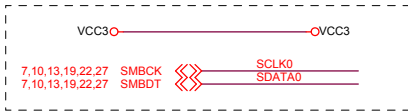


DDR3-240P-OR

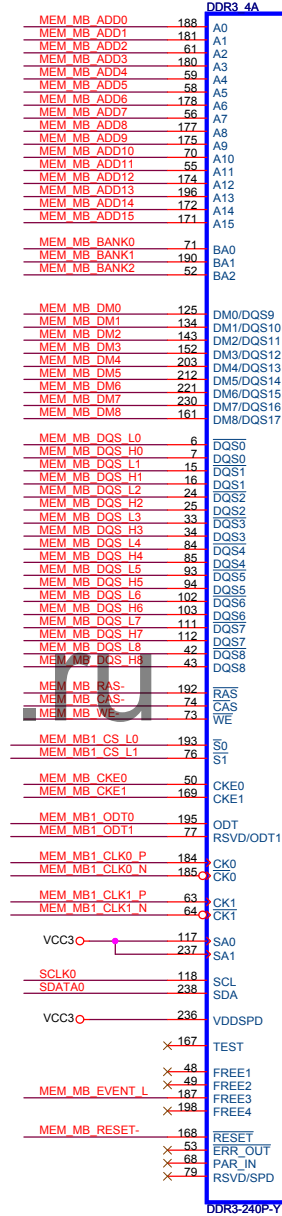


DDR3-240P-Y



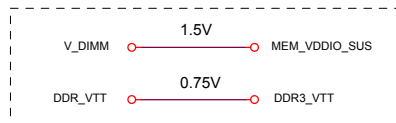


DDR3-240P-OR

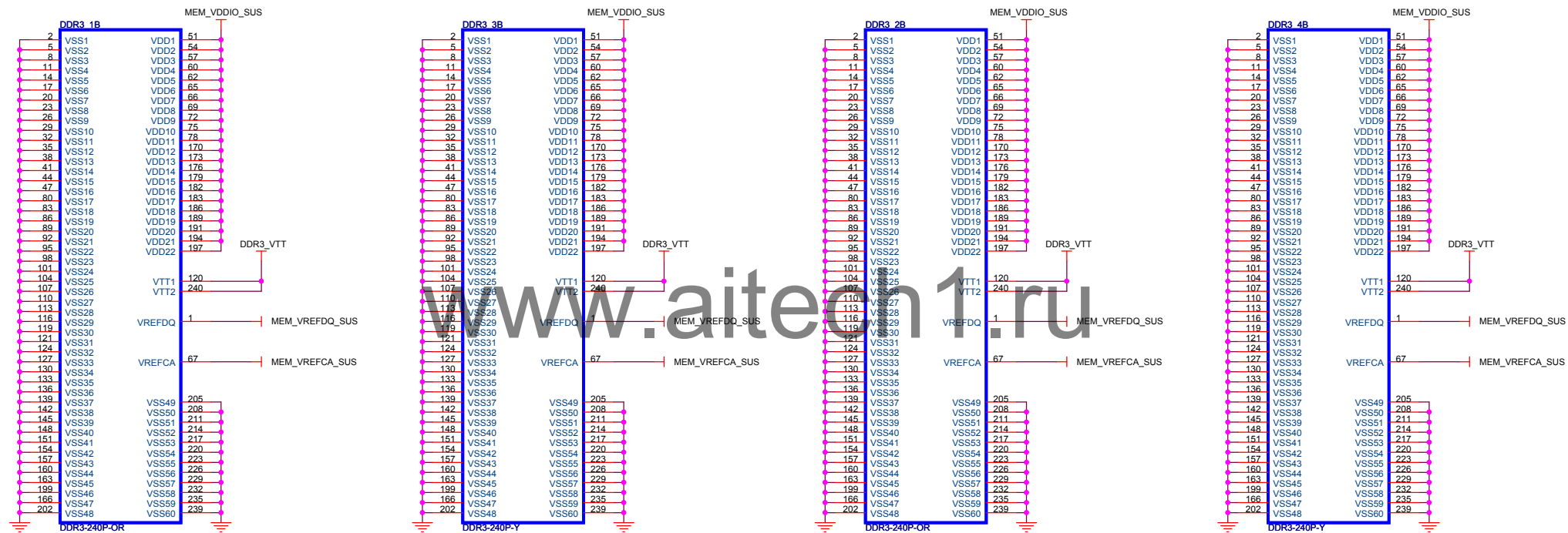
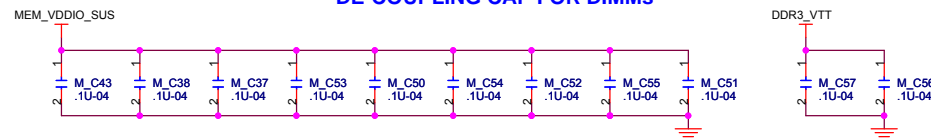


DDR3-240P-Y

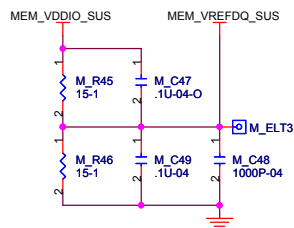




## DE-COUPLING CAP FOR DIMMs

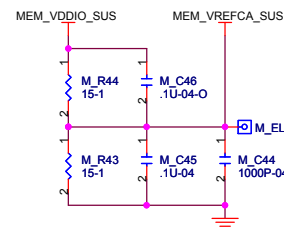


## MEM\_VREFDQ\_SUS



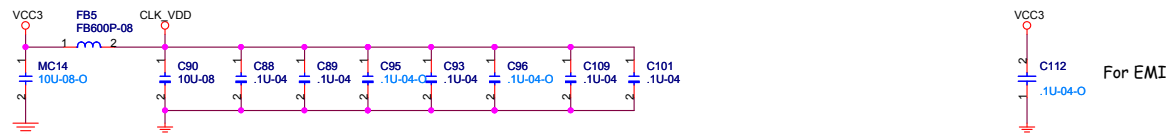
Layout: Place within 500 mils of the DIMMB1 socket.  
12mil(width);20mil(spacing)

## MEM\_VREFCA\_SUS



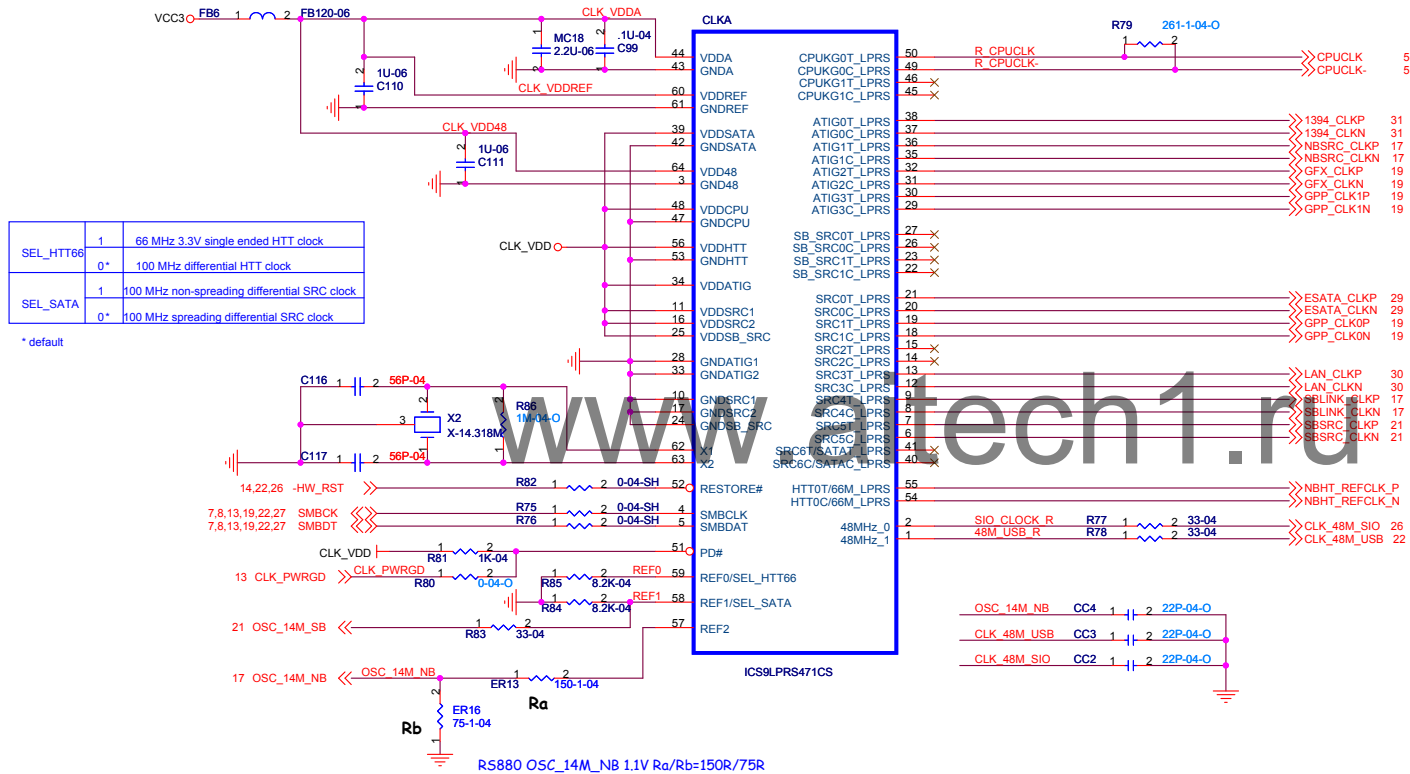
Layout: Place within 500 mils of the DIMMB1 socket.  
12mil(width);20mil(spacing)





1- PLACE ALL SERIAL TERMINATION  
RESISTORS CLOSE TO CLOCK GEN

2- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



For 1394  
NB PCI-E GFX CLK  
For GFX SLOT  
For PCIE2 SLOT

For ESATA  
For PCIE1 SLOT

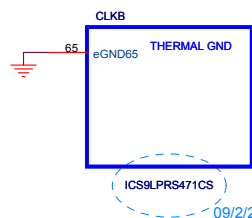
For LAN CHIP  
For A-Link(NB)  
For A-Link(SB)

HT REF CLK

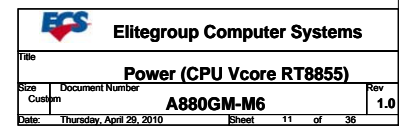
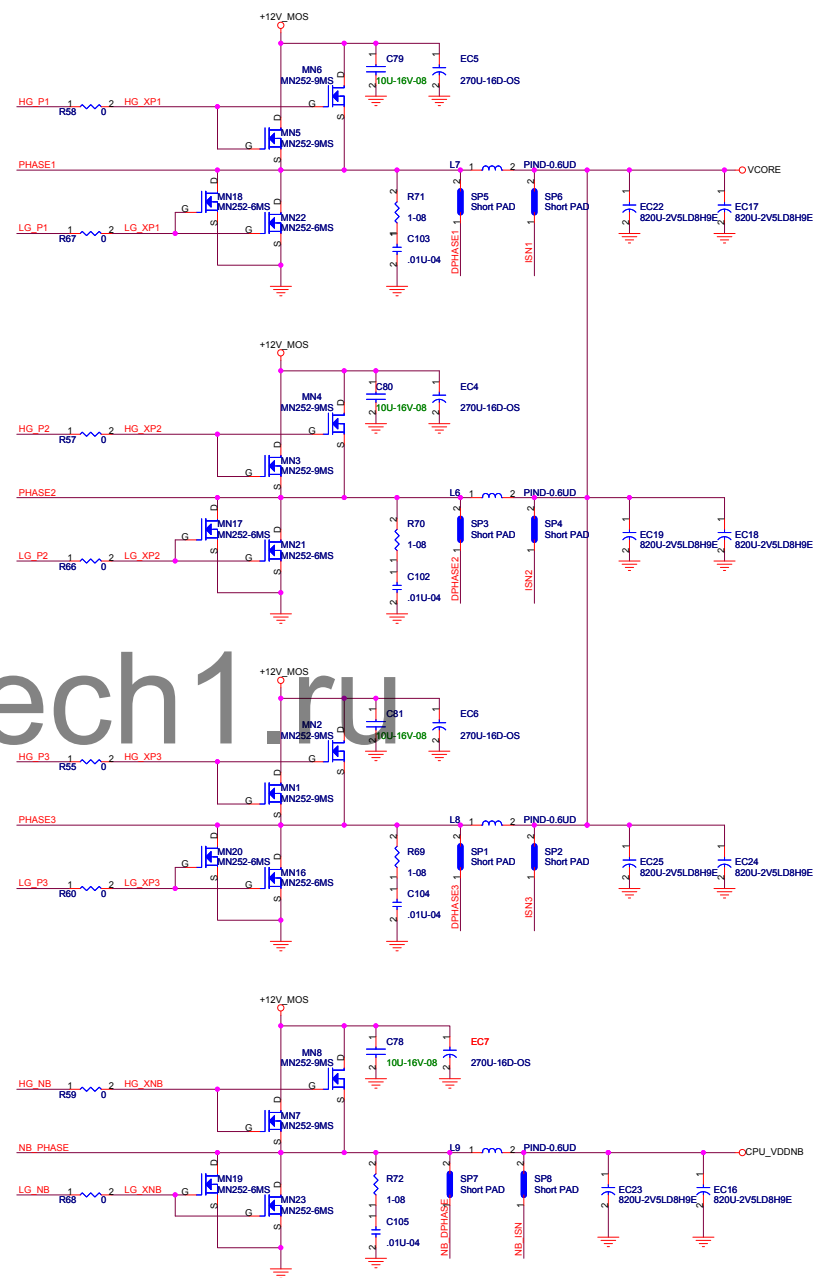
NB CLOCK INPUT TABLE

NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	VREF
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

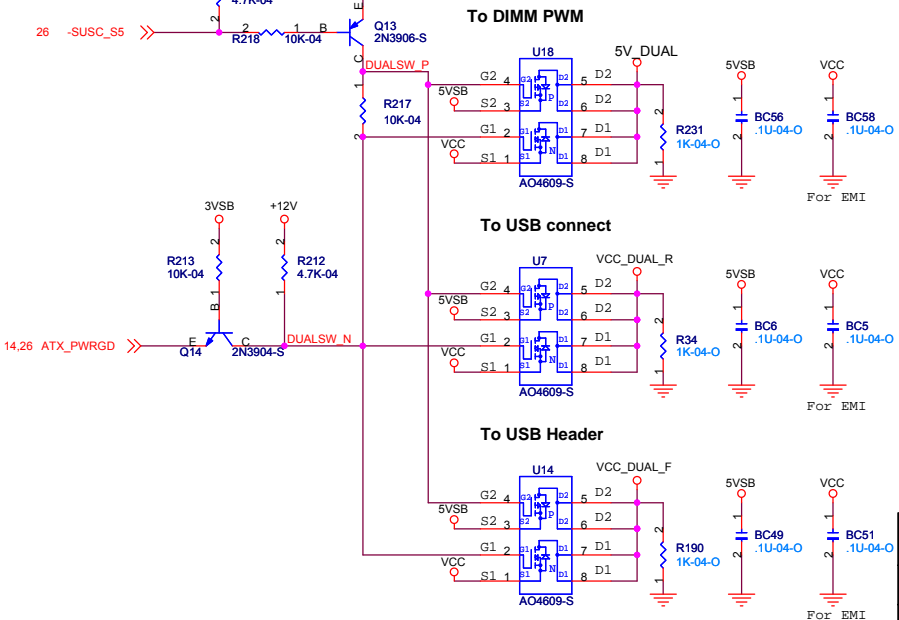
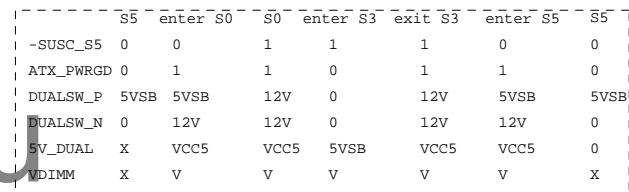
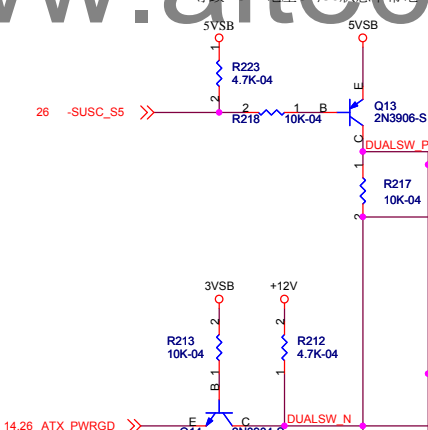
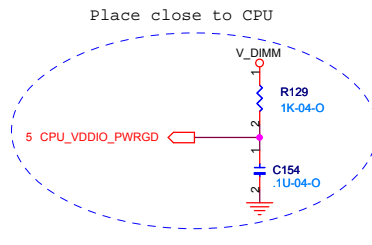
\* RS880 can be used as clock buffer to output two PCIE reference clocks  
By default, chip will configured as input mode, BIOS can program it to output mode.  
Clock chip has internal serial terminations for differential pairs









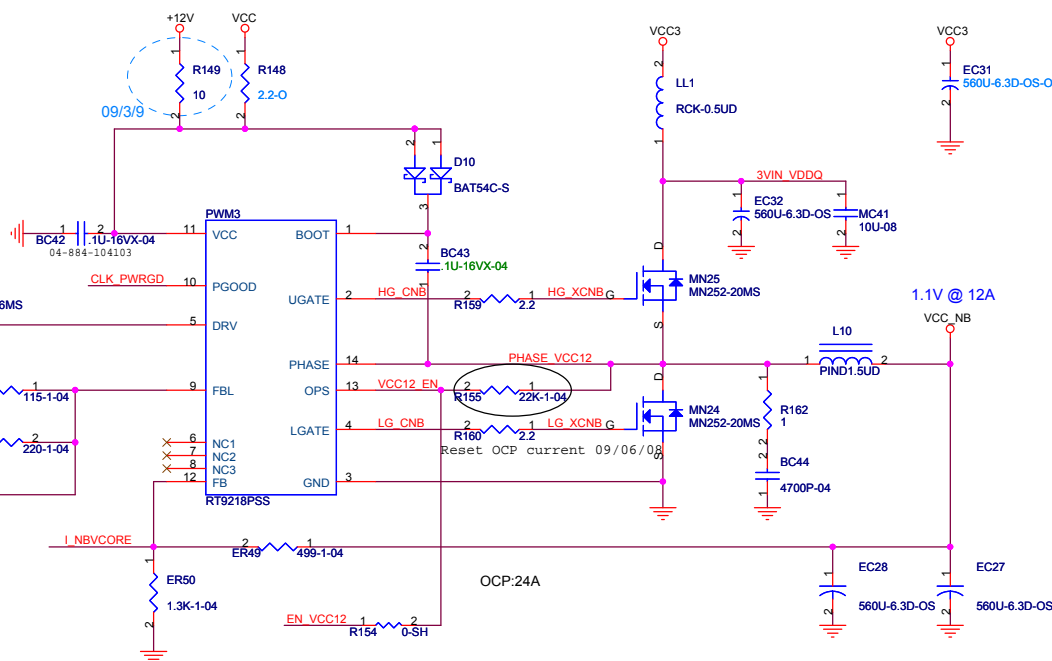




26 EN\_VCC12 >> EN\_VCC12  
10 CLK\_PWRGD << CLK\_PWRGD

SIO_GP20	SIO_GP21	V_DIMM
1	1	1.20V
0	1	1.25V
1	0	1.30V
0	0	1.35V

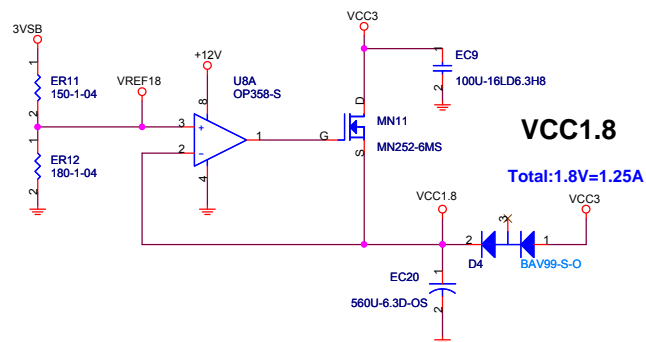
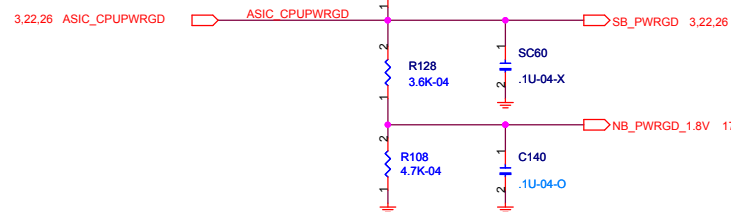
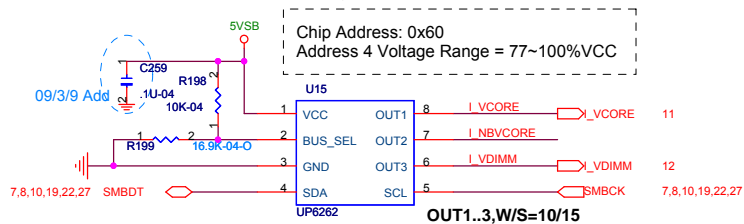
Total: 1.2V=5.5A  
1.2V @ 3.6A  
1.2V @ 1.9A  
Place close to CPU  
09/2/20



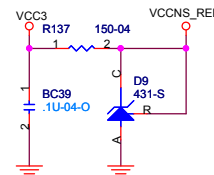
uP6262的電流輸出與 $\Delta V_{out}$ 的關係如下:  
選取從uP6262輸出的方向為正,  
則 $V_{CORE}$ ,  $V_{CC\_NB}$ 及 $V_{DIMM}$ 的 $\Delta V_{out}$ 為:  
 $\Delta V_{out} = -I_c \cdot R_{FB}$ ;

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SB&NB PWRGOOD



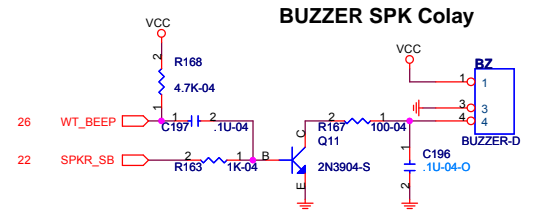
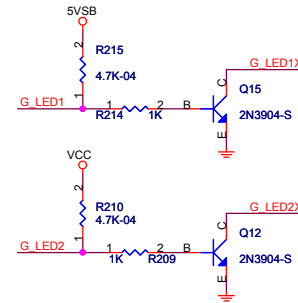
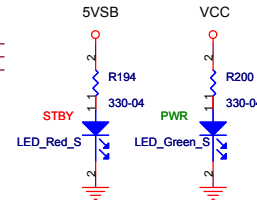
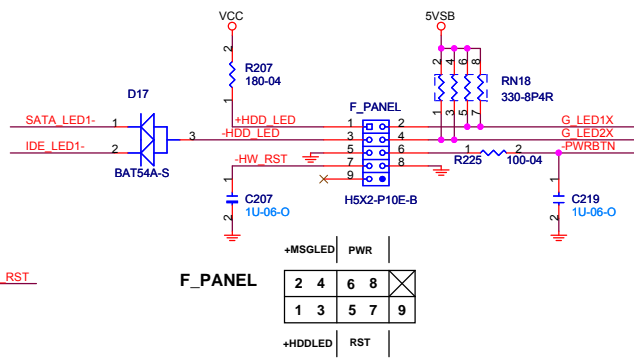
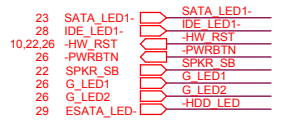
For CPU VDDA reference





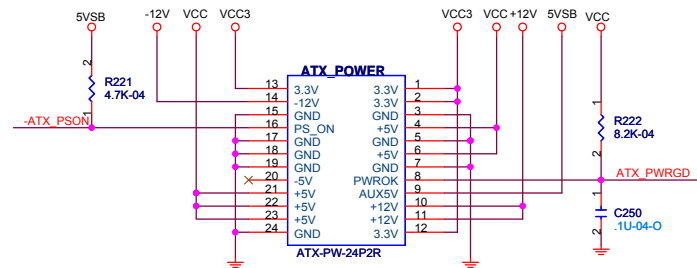
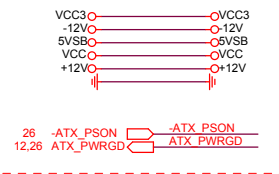
## FRONT PANEL

### External Connection

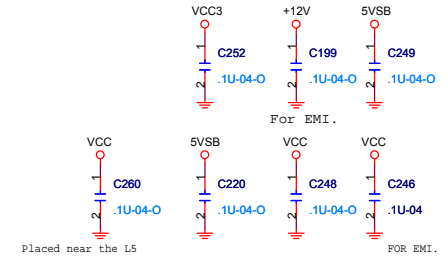
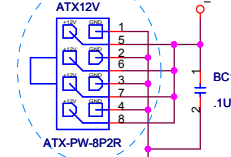


## POWER CONNECTOR

### External Connection

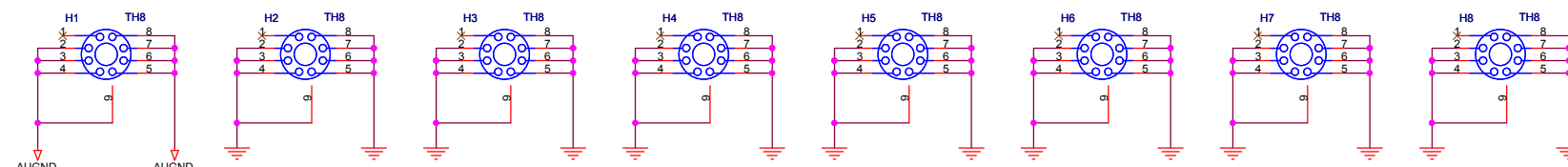
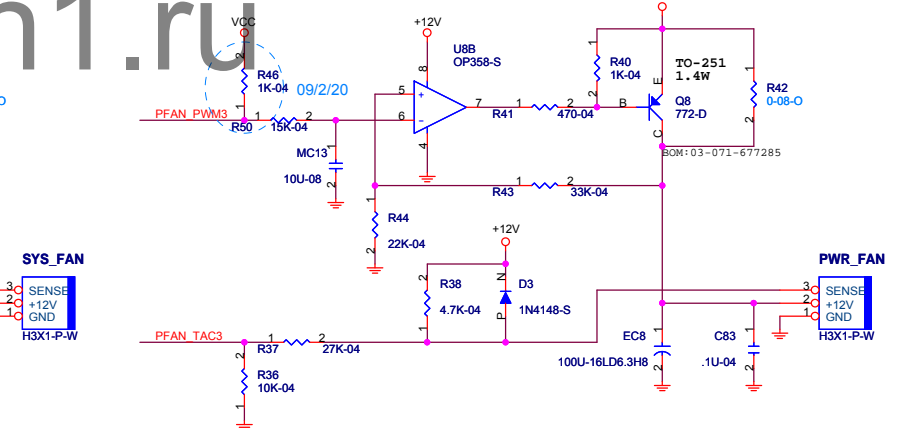
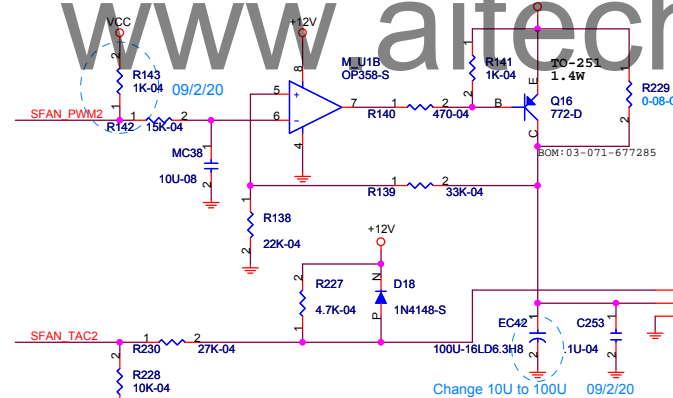
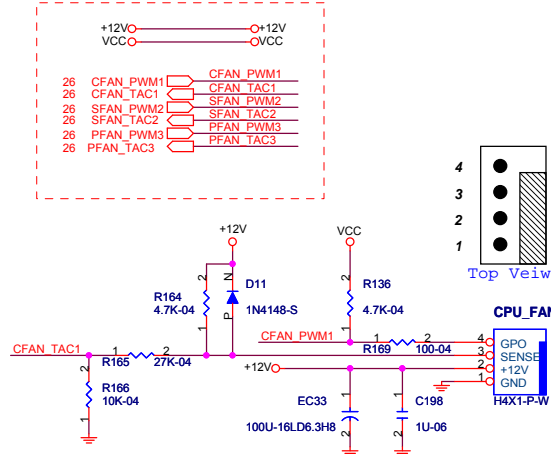
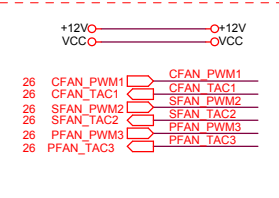


Change to 8pin power connector  
09/2/20



## FAN

### External Connection





# HT LINK

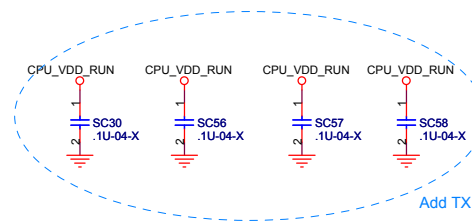
- 3 HT\_CLKIN\_H[0..1] >> HT\_CLKIN\_P[0..1]
- 3 HT\_CLKIN\_L[0..1] >> HT\_CLKIN\_N[0..1]
- 3 HT\_CLKOUT\_H[0..1] << HT\_CLKOUT\_P[0..1]
- 3 HT\_CLKOUT\_L[0..1] << HT\_CLKOUT\_N[0..1]
- 3 HT\_CTLIN\_H[0..1] >> HT\_CTLIN\_P[0..1]
- 3 HT\_CTLIN\_L[0..1] >> HT\_CTLIN\_N[0..1]
- 3 HT\_CTLOUT\_H[0..1] << HT\_CTLOUT\_P[0..1]
- 3 HT\_CTLOUT\_L[0..1] << HT\_CTLOUT\_N[0..1]
- 3 HT\_CADIN\_H[0..15] >> HT\_CADIN\_P[0..15]
- 3 HT\_CADIN\_L[0..15] >> HT\_CADIN\_N[0..15]
- 3 HT\_CADOUT\_H[0..15] << HT\_CADOUT\_P[0..15]
- 3 HT\_CADOUT\_L[0..15] << HT\_CADOUT\_N[0..15]

HT CADOUT P0	Y25	HT RXCADP0
HT CADOUT N0	Y24	HT RXCADN0
HT CADOUT P1	Y25	HT RXCADP1
HT CADOUT N1	Y23	HT RXCADN1
HT CADOUT P2	Y25	HT RXCADP2
HT CADOUT N2	Y25	HT RXCADN2
HT CADOUT P3	U24	HT RXCADP3
HT CADOUT N3	U25	HT RXCADN3
HT CADOUT P4	T25	HT RXCADP4
HT CADOUT N4	T24	HT RXCADN4
HT CADOUT P5	P25	HT RXCADP5
HT CADOUT N5	P23	HT RXCADN5
HT CADOUT P6	P25	HT RXCADP6
HT CADOUT N6	P24	HT RXCADN6
HT CADOUT P7	N24	HT RXCADP7
HT CADOUT N7	N25	HT RXCADN7
HT CADOUT P8	AC24	HT RXCADBP8
HT CADOUT N8	AC25	HT RXCADBN8
HT CADOUT P9	AB25	HT RXCADBP9
HT CADOUT N9	AB24	HT RXCADBN9
HT CADOUT P10	AA24	HT RXCADBP10
HT CADOUT N10	AA25	HT RXCADBN10
HT CADOUT P11	Y22	HT RXCADP11
HT CADOUT N11	Y23	HT RXCADN11
HT CADOUT P12	W21	HT RXCADP12
HT CADOUT N12	W20	HT RXCADN12
HT CADOUT P13	V21	HT RXCADP13
HT CADOUT N13	V20	HT RXCADN13
HT CADOUT P14	U21	HT RXCADP14
HT CADOUT N14	U20	HT RXCADN14
HT CADOUT P15	U19	HT RXCADP15
HT CADOUT N15	U18	HT RXCADN15
HT CLKOUT P0	T22	HT RXCLKP0
HT CLKOUT N0	T23	HT RXCLKN0
HT CLKOUT P1	AB23	HT RXCLKP1
HT CLKOUT N1	AA22	HT RXCLKN1

## HYPER TRANSPORT CPU I/F

HT_TXCAD09P	D24	HT CADIN P0
HT_TXCAD01P	D25	HT CADIN N0
HT_TXCAD1P	E24	HT CADIN P1
HT_TXCAD10P	E25	HT CADIN N1
HT_TXCAD2P	F24	HT CADIN P2
HT_TXCAD20P	F25	HT CADIN N2
HT_TXCAD3P	E23	HT CADIN P3
HT_TXCAD30P	F22	HT CADIN N3
HT_TXCAD4P	H23	HT CADIN P4
HT_TXCAD40P	I22	HT CADIN N4
HT_TXCAD5P	J25	HT CADIN P5
HT_TXCAD50P	J24	HT CADIN N5
HT_TXCAD6P	K24	HT CADIN P6
HT_TXCAD60P	K25	HT CADIN N6
HT_TXCAD7P	K23	HT CADIN P7
HT_TXCAD70P	K22	HT CADIN N7
HT_TXCAD8P	F21	HT CADIN P8
HT_TXCAD80P	G21	HT CADIN N8
HT_TXCAD9P	G20	HT CADIN P9
HT_TXCAD90P	J20	HT CADIN N9
HT_TXCAD10P	J21	HT CADIN P10
HT_TXCAD11P	J18	HT CADIN N10
HT_TXCAD11P	K17	HT CADIN P11
HT_TXCAD12P	I19	HT CADIN N11
HT_TXCAD12P	J19	HT CADIN P12
HT_TXCAD12N	M19	HT CADIN P13
HT_TXCAD13P	L18	HT CADIN N13
HT_TXCAD13P	M21	HT CADIN P14
HT_TXCAD14P	M20	HT CADIN N14
HT_TXCAD14P	P18	HT CADIN P15
HT_TXCAD15P	M18	HT CADIN N15
HT_TXCAD15N		
HT_TXCLK0P	H24	HT CLKIN P0
HT_TXCLK0N	H25	HT CLKIN N0
HT_TXCLK1P	L21	HT CLKIN P1
HT_TXCLK1N	L20	HT CLKIN N1
HT_TXCLK1N		
HT_TXCTL0P	M24	HT CTLIN P0
HT_TXCTL0N	E19	HT CTLIN N0
HT_TXCTL1P	F18	HT CTLIN P1
HT_TXCTL1N	E18	HT CTLIN N1
HT_TXCALP	B24	HT CALIN P0
HT_TXCALN	B25	HT CALIN N0

H24	HT_CLKIN_P0	
H25	HT_CLKIN_N0	
L21	HT_CLKIN_P1	
L20	HT_CLKIN_N1	
M24	HT_CTLIN_P0	
M25	HT_CTLIN_N0	
P19	HT_CTLIN_P1	
R18	HT_CTLIN_N1	
B24	HT_TXCALP	1
B25	HT_TXCALN	ER3





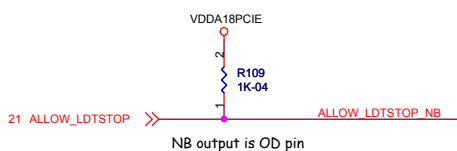
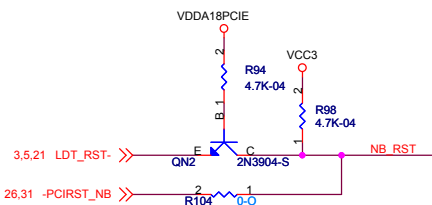
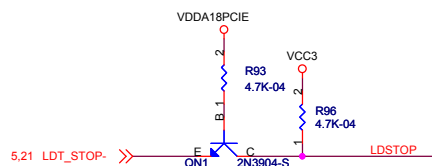




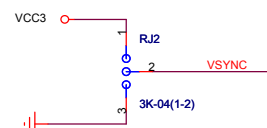
# RS880 Control signal

POWERGOOD	1.8V IN
ALLOW_LDTSTOP	1.8V IN
LDT_STOP#	3.3V IN/OD
IN(default)/OUT	SYSTEMRESETb
SYSTEMRESETb	IN

\* CLMC mode: NB send LDT\_STOP#, ALLOW\_LDTSTOP will become input



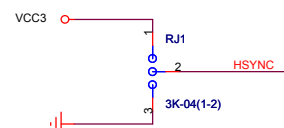
## RS880: Debug Test Bus(1,Disable)



## RS880: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

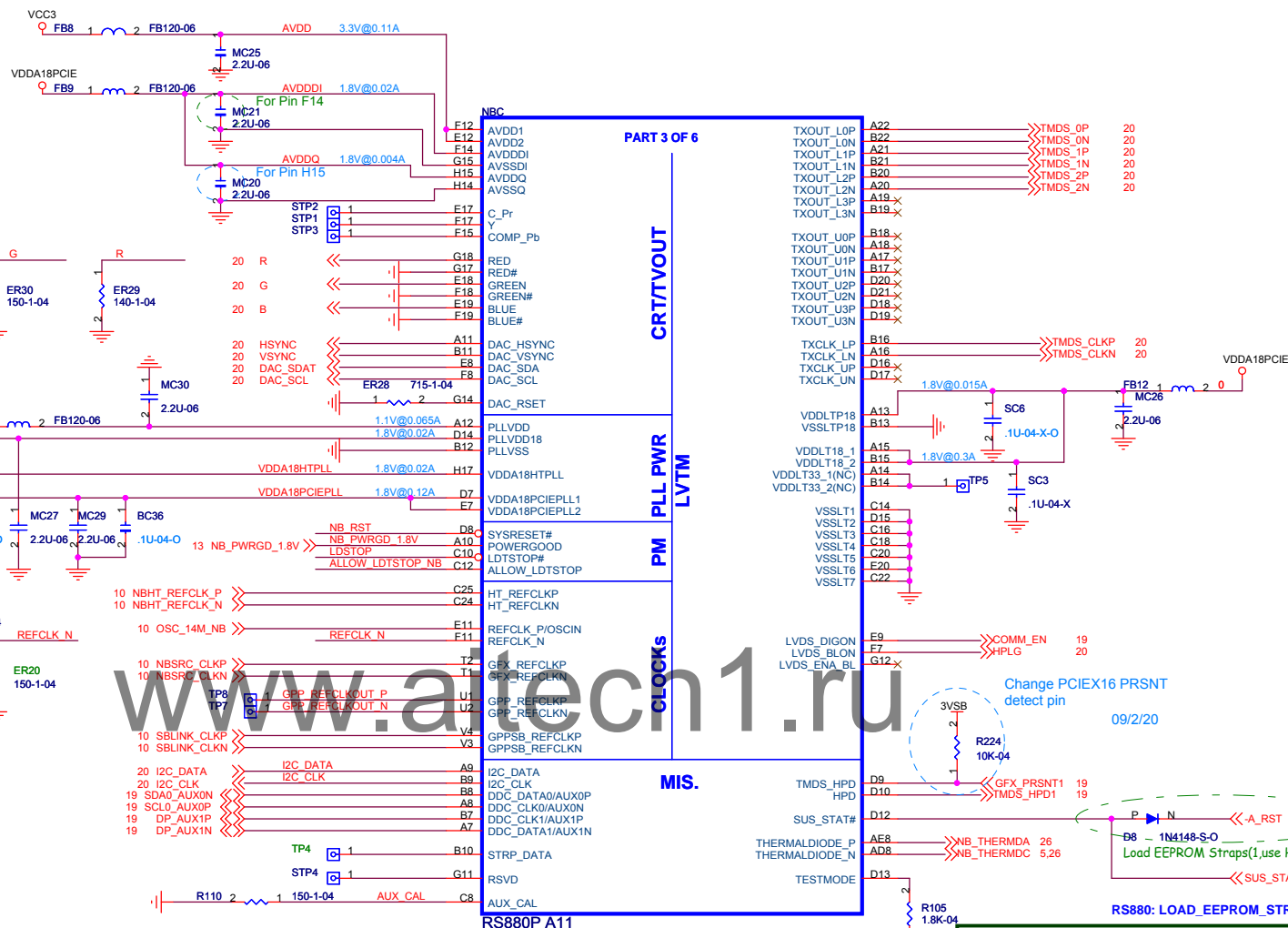
Enables the Test Debug Bus using GPIO.  
1 : Disable  
0 : Enable

## RS880: Enable side port memory(1,Disable)



## RS880: Enables Side port memory

Selects if Memory SIDE PORT is available or not  
1 = Memory Side port Not available  
0 = Memory Side port available  
Register Readback of strap:  
NB\_CLKCFG:CLK\_TOP\_SPARE\_D[1]



## RS880: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected







# PCI EXPRESS\_x16

# PCI\_EXPRESS\_x1



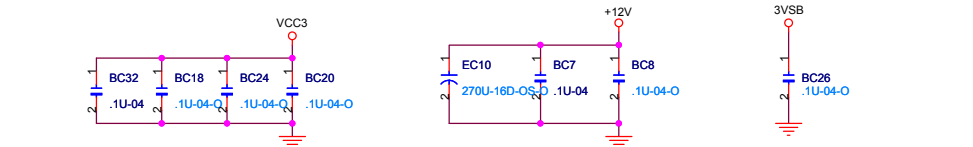
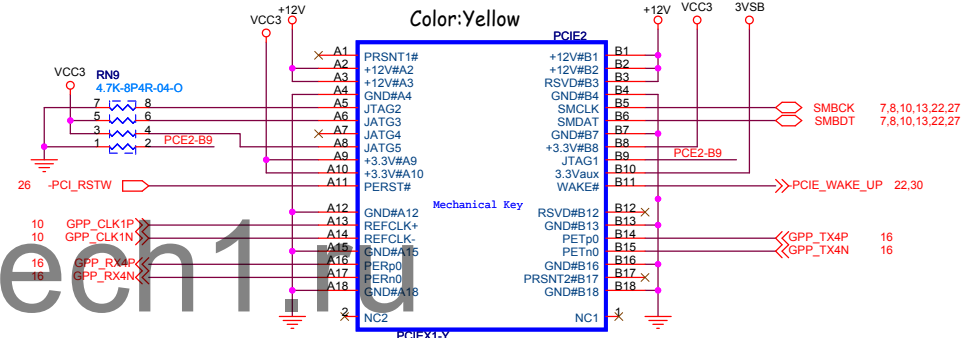
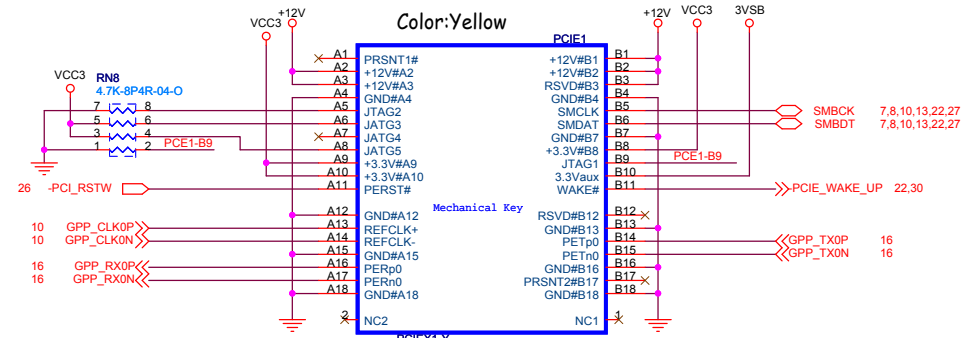
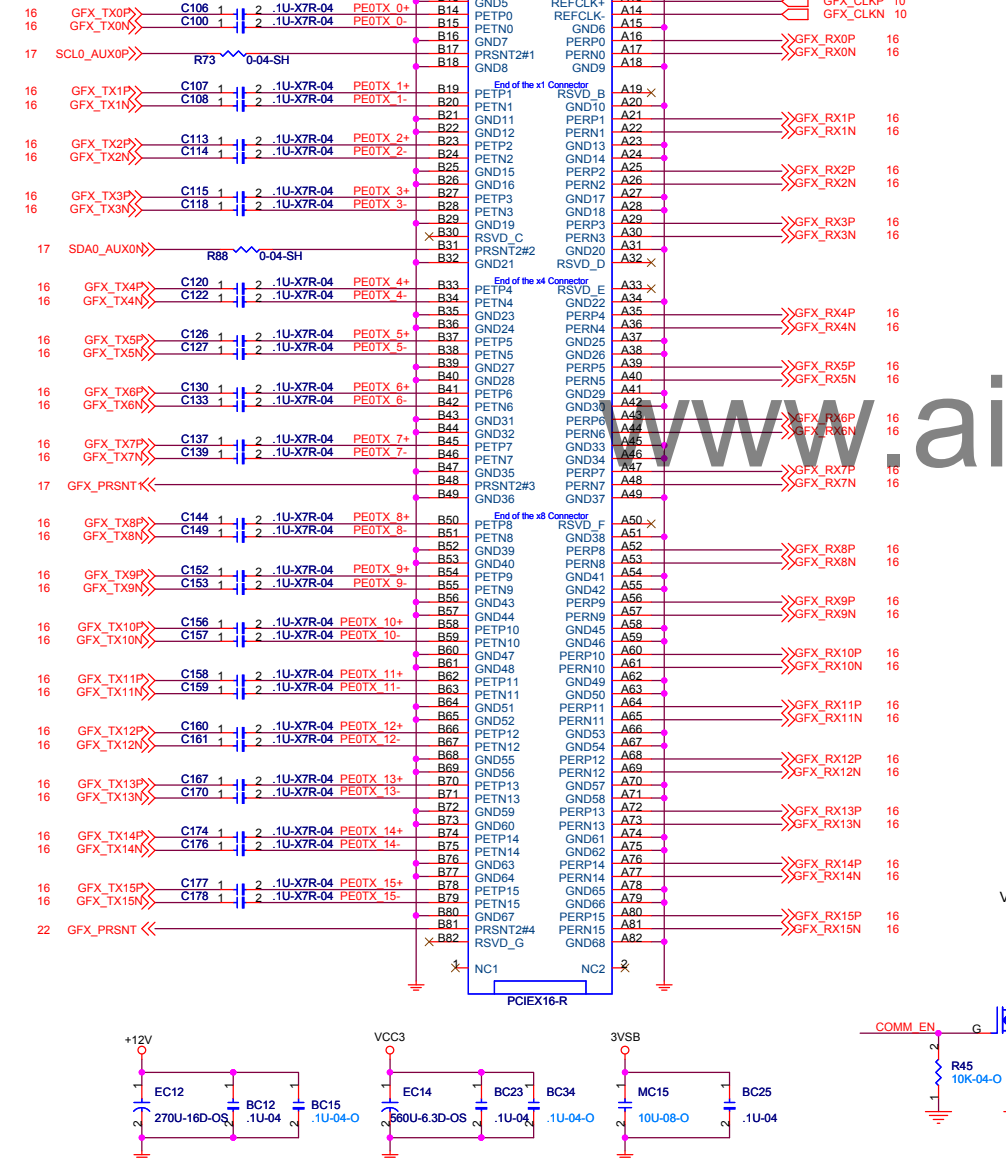
PLACE THESE CAP  
CLOSE TO CONNECTOR

Color:Orange

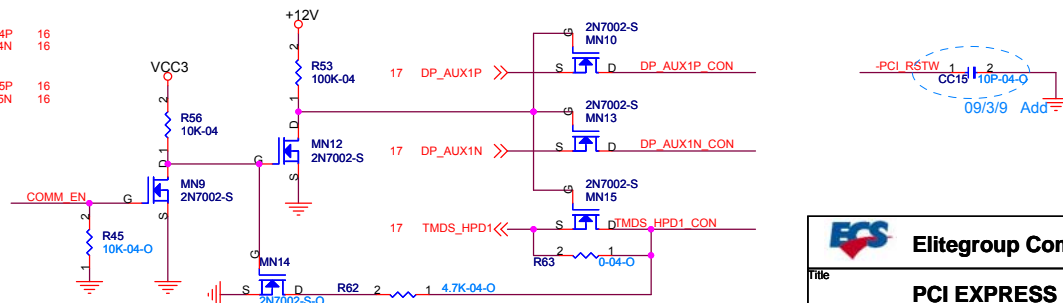
+12V:5.5Amp

Color:Yellow

## Refer Demo Board



## SWITCH CIRCUIT FOR SECONDARY DISPLAYPORT





VCC

VCC3\_SW

17 HPLG

17 I2C\_CLK

17 I2C\_DATA

17 TMSD\_0P

17 TMSD\_0N

17 TMSD\_1P

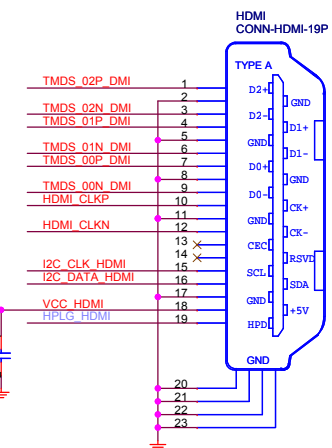
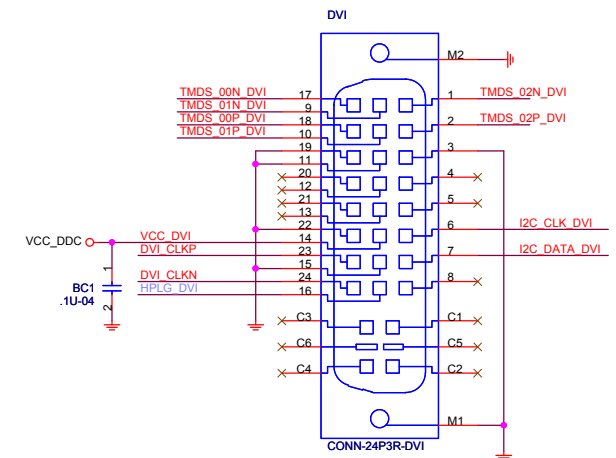
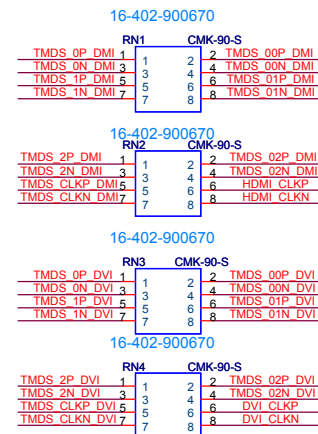
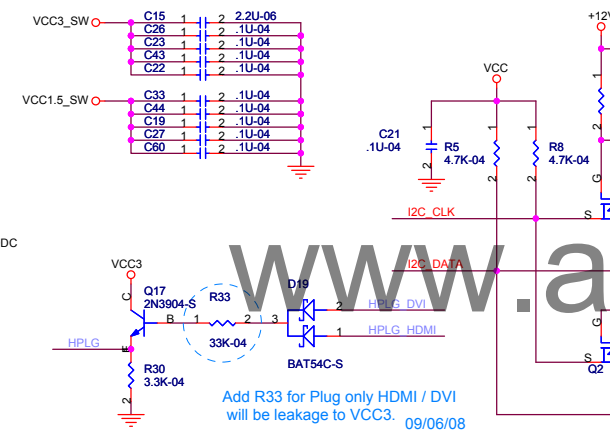
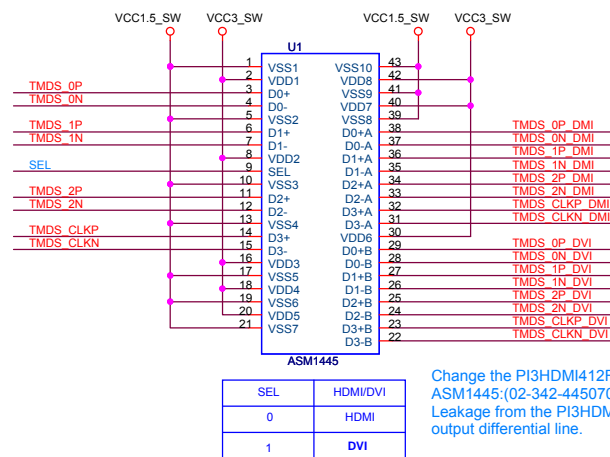
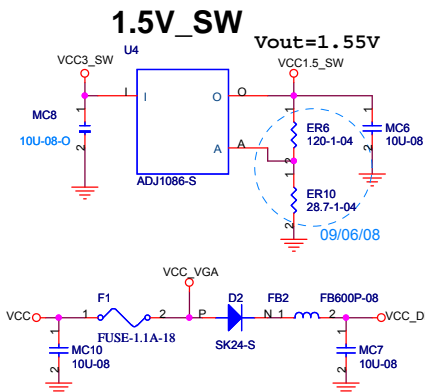
17 TMSD\_1N

17 TMSD\_2P

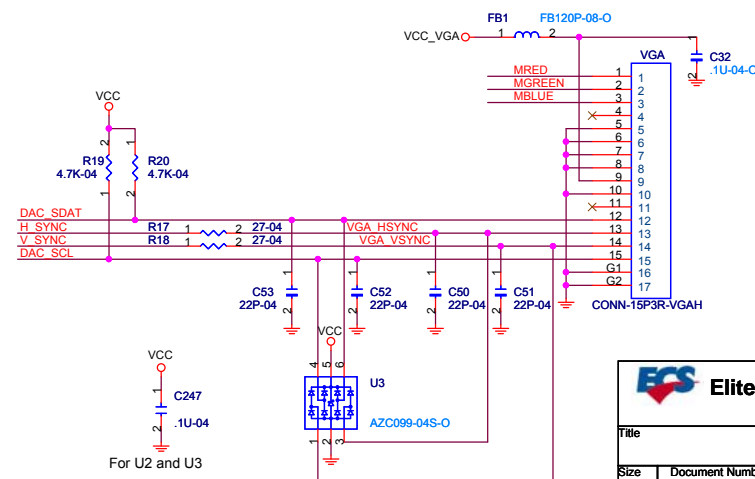
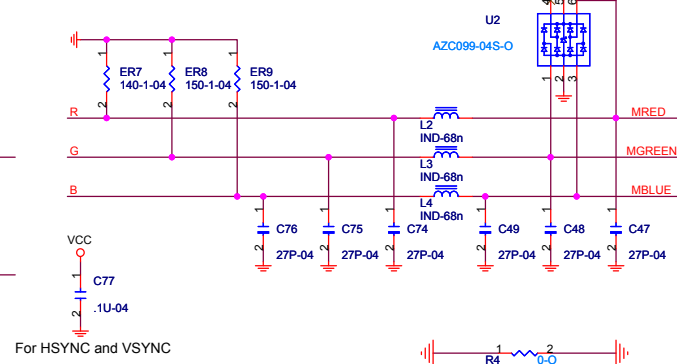
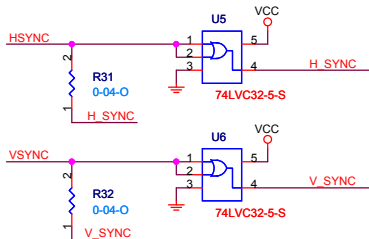
17 TMSD\_2N

17 TMSD\_CLKP

17 TMSD\_CLKN

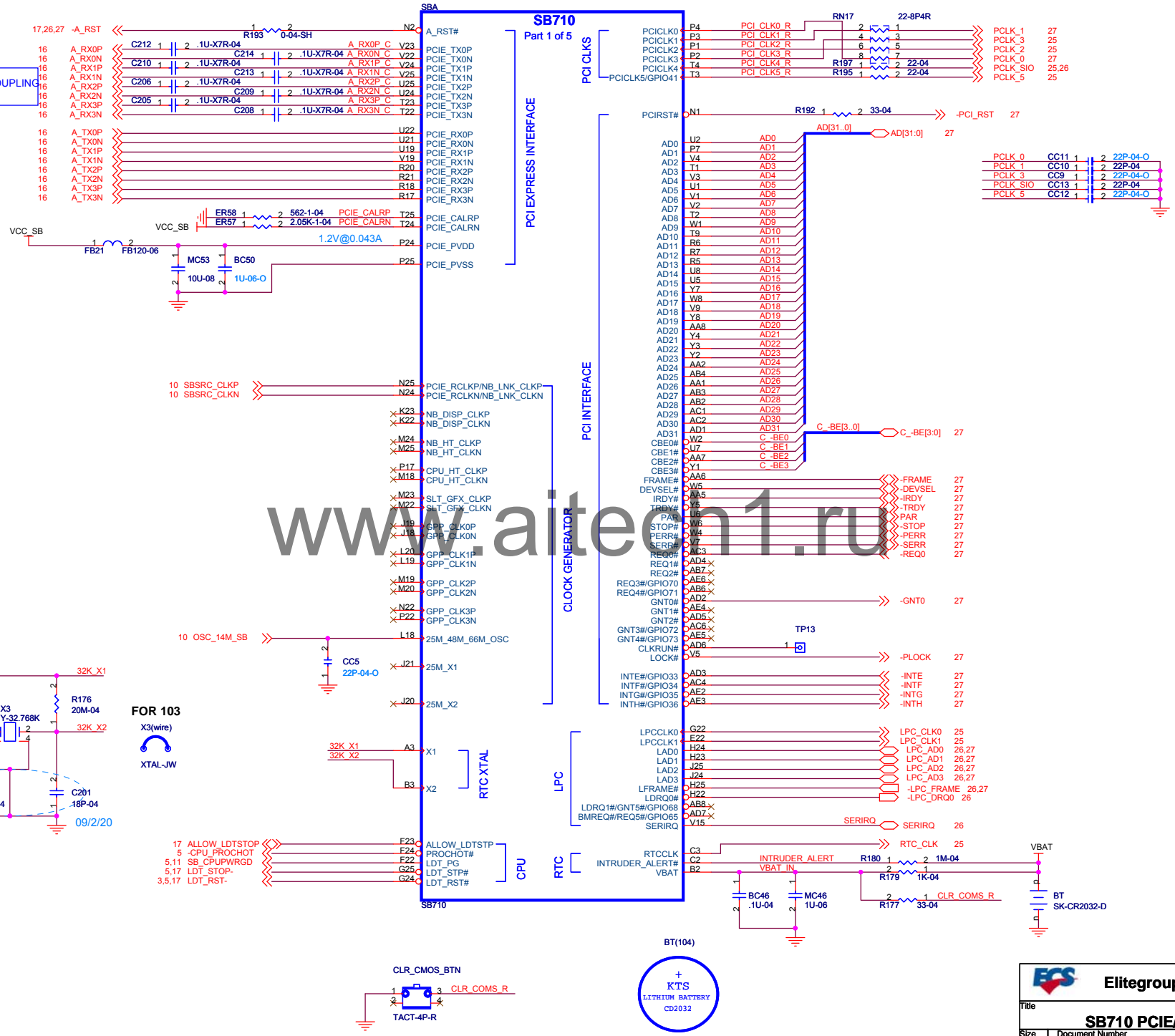


17	HSYNC	HSYNC
17	VSYNC	VSYNC
17	R	R
17	G	G
17	B	B
17	DAC_SDAT	DAC_SDAT
17	DAC_SCL	DAC_SCL



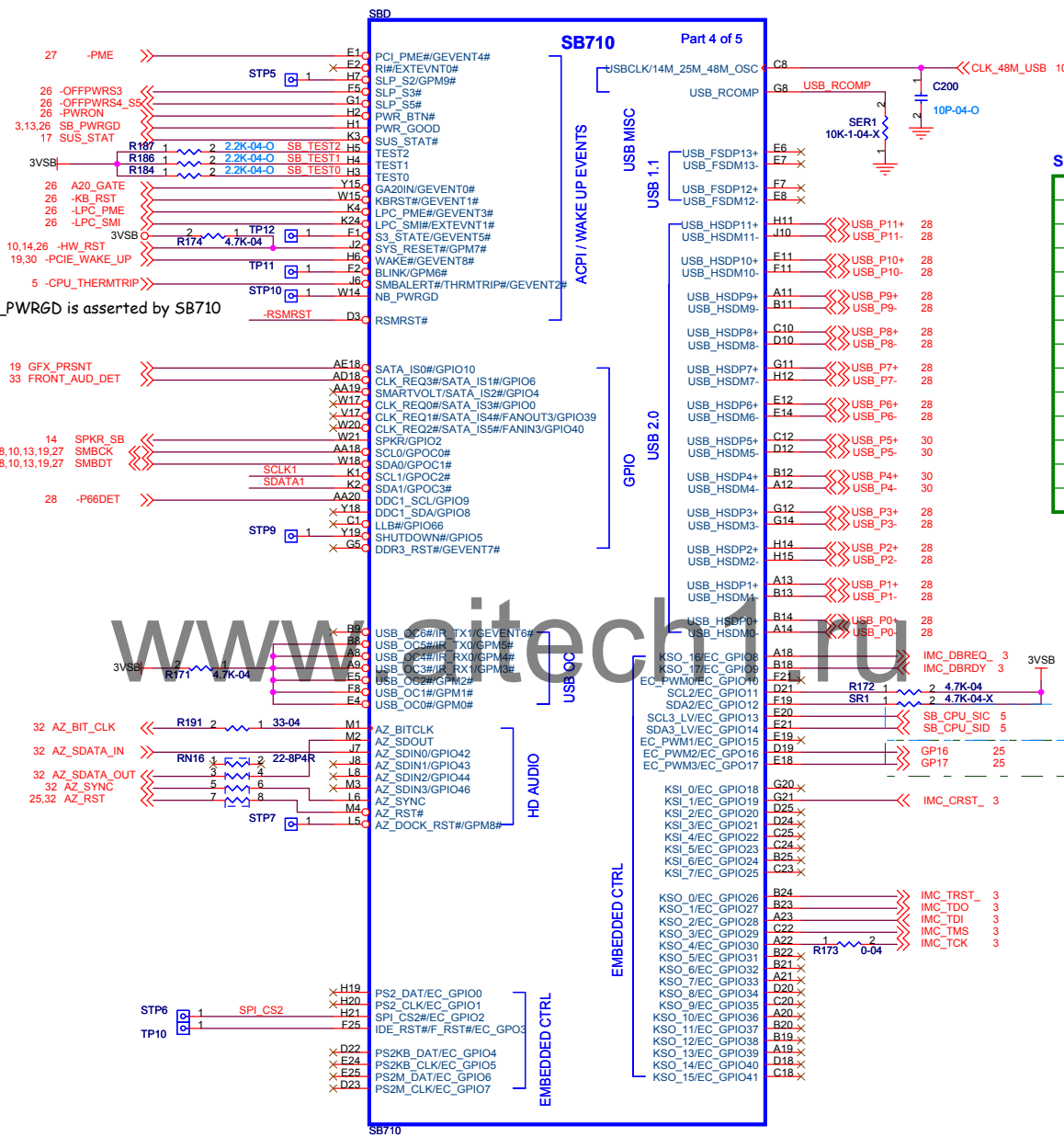
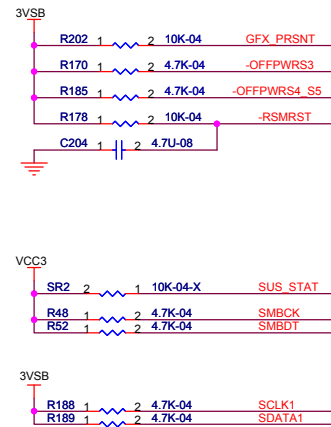


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO BGA





If use internal CLK GEN NB\_PWRGD is asserted by SB710



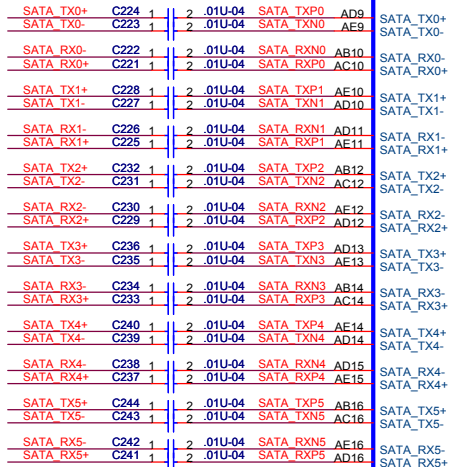
SB710 POWER TABLE

PIN NAME	SB710	PIN NAME	SB710
VCC_SB: 1.2V		VCC3	
PCIE_PVDD	0.043A	XTLVDD_SATA	0.006A
PLLVD_SATA	0.093A	VDDQ	0.131A
PCIE_VDDR	0.6A	VDD33_18	0.071A
AVDD_SATA	0.567A	AVDDCK_3.3V	0.047A
VDD	0.51A	Total	0.255A
CKVDD_1.2V		3VSB	
AVDDCK_1.2V	0.062A	AVDDTX/RX	0.658A
Total	1.875A	AVDDC	0.017A
1.2VSB		S5_3.3V	0.032A
S5_1.2V	0.113A	Total	0.707A
USB_PHY_1.2V	0.197A	5VSB	
Total	0.31A	V5_VREF	0.001A

09/02/20  
SMBus Clk 3 for  
CPU temp status  
STRAP pin to define  
use LPC or SPI ROM

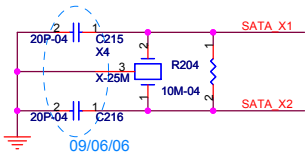


PLACE SATA AC COUPLING  
CAPS CLOSE TO SB710



PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF SB710

**NOTE:**  
SER2 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



## SB710 Part 2 of 5

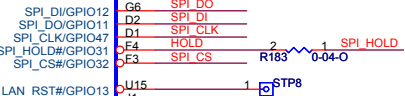
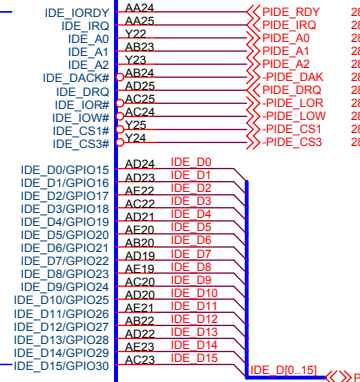
SERIAL ATA

ATA 66/100/133

SPI ROM

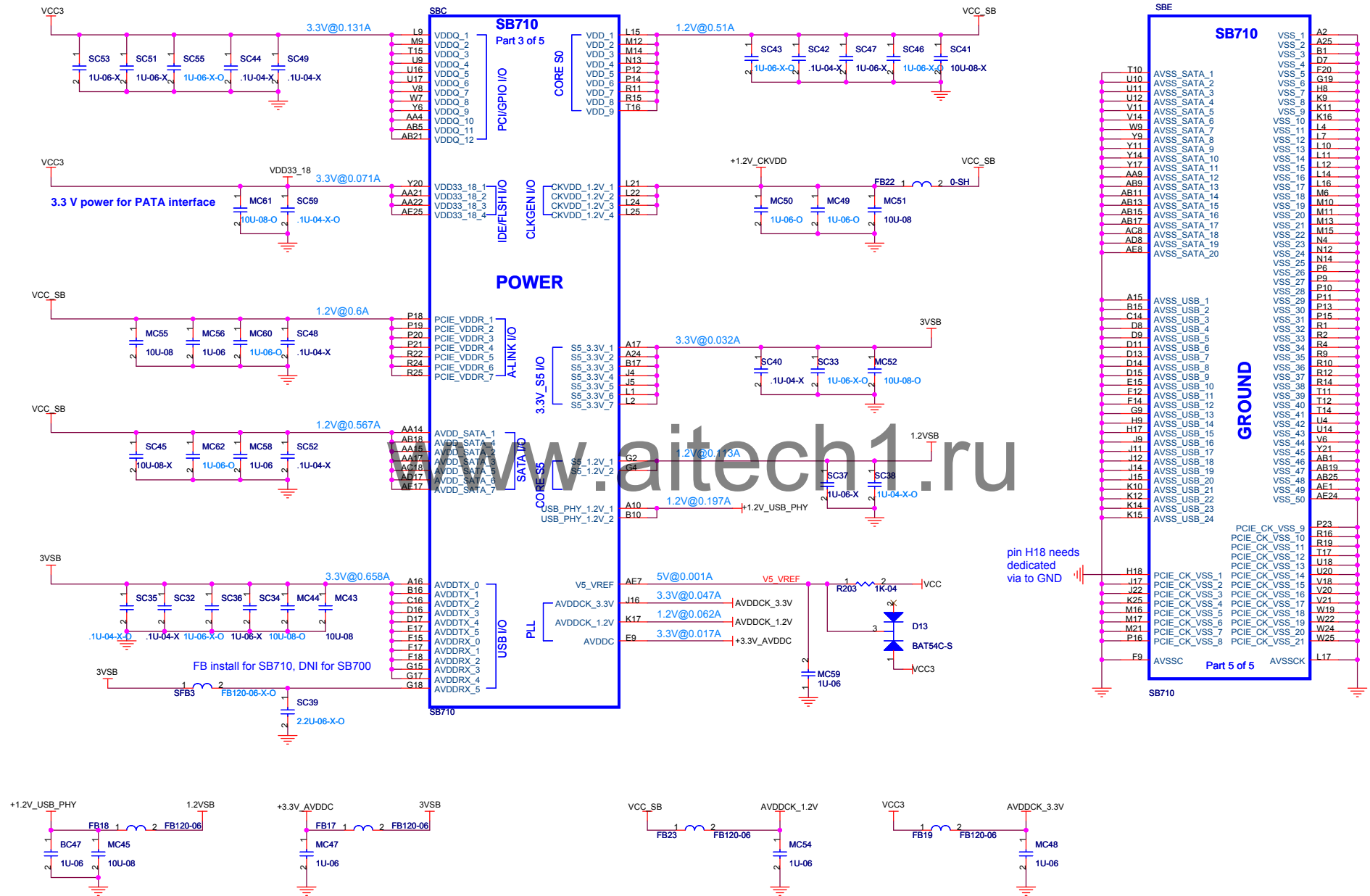
HW MONITOR

SATA PWR



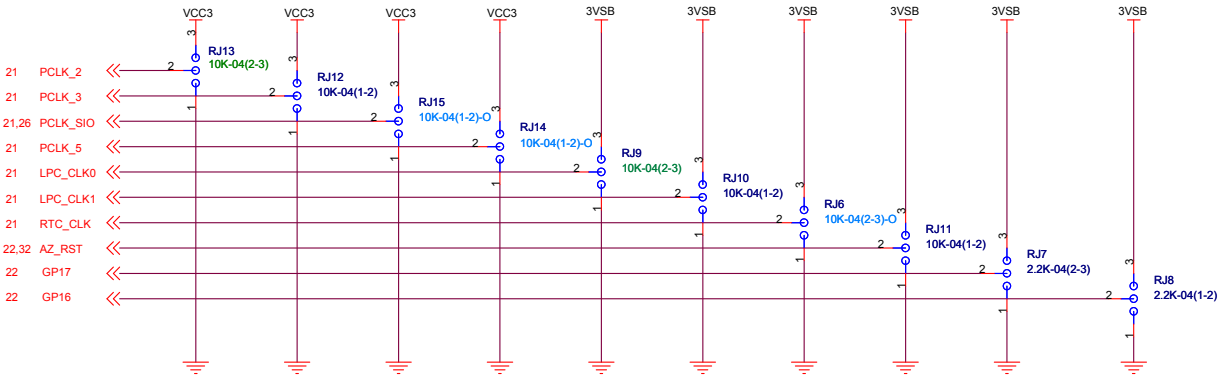


PLACE ALL THE DECOUPLING CAPS ON  
THIS SHEET CLOSE TO SB AS POSSIBLE.



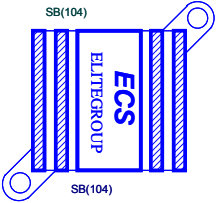


NOTE: SB710 HAS INTERNAL 10K PULL UP RESISTOR FOR RTC\_CLK



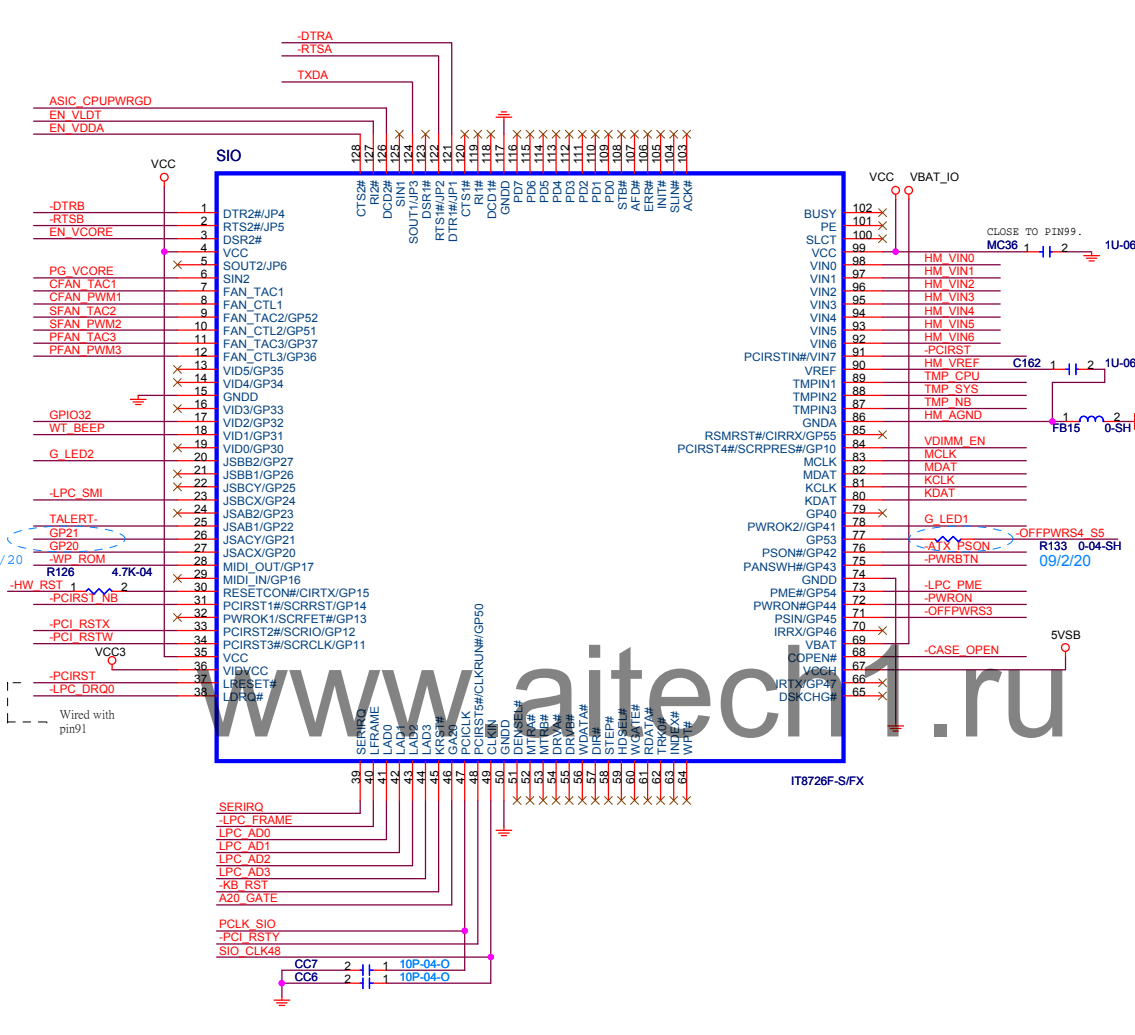
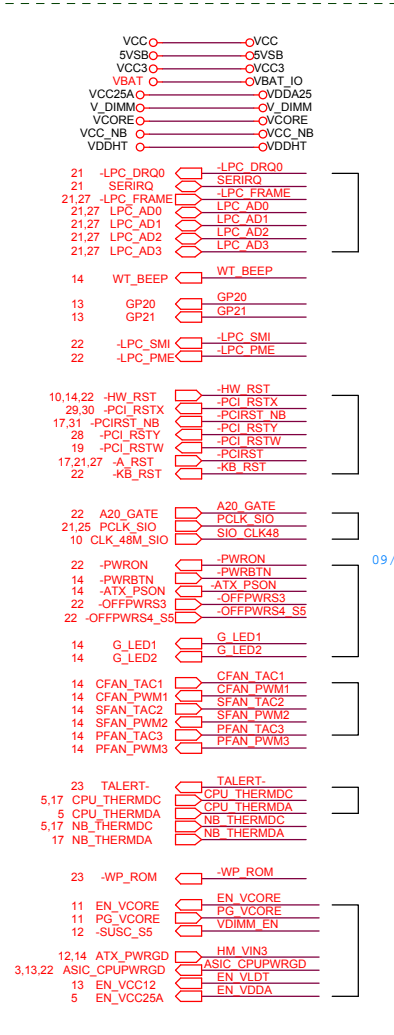
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	Watchdog ENABLED DEFAULT	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable DEFAULT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM DEFAULT	
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS DEFAULT			IMC Disable	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable DEFAULT		

REQUIRED STRAPS



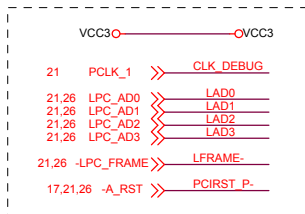


## External Connection

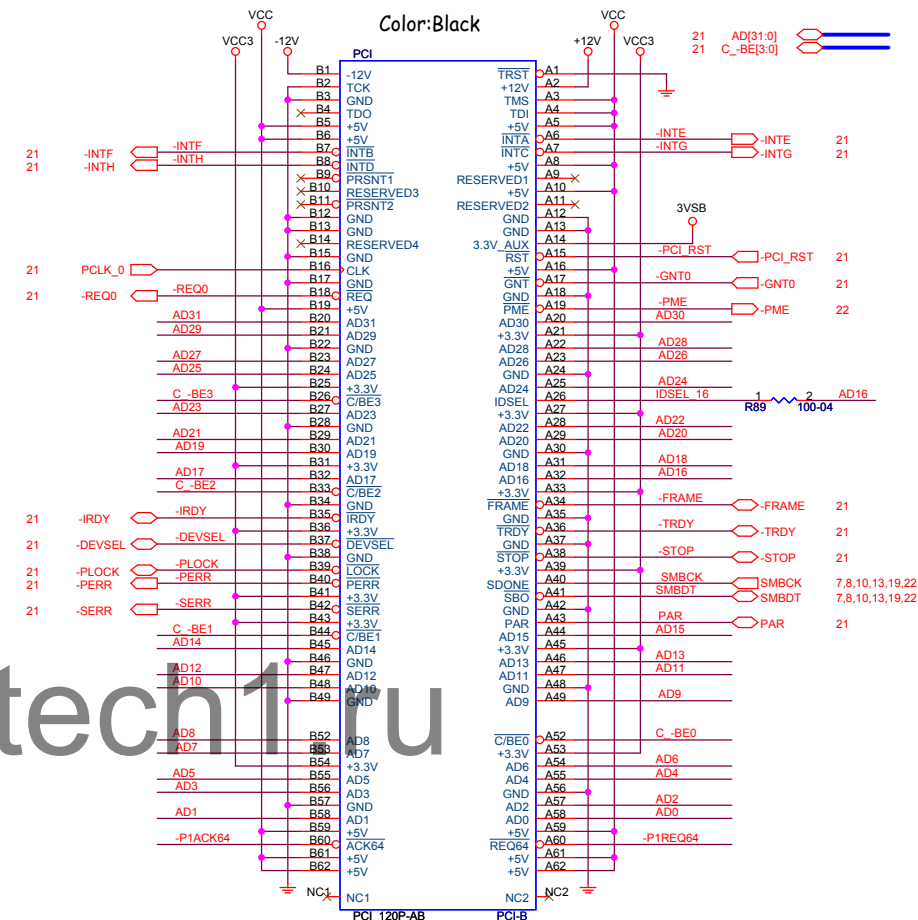
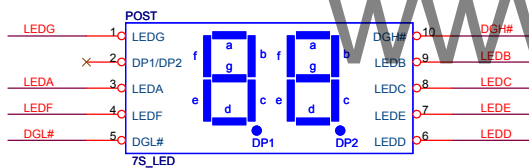
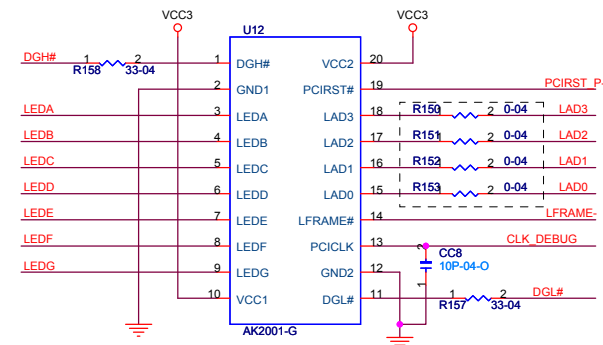
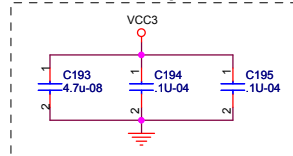




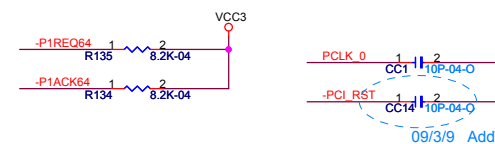
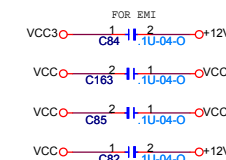
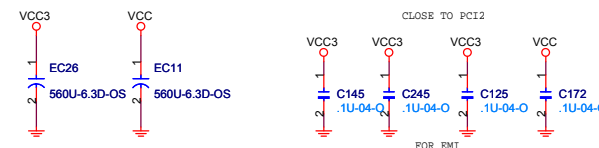
## External Connection



## Close to U12 power Pin



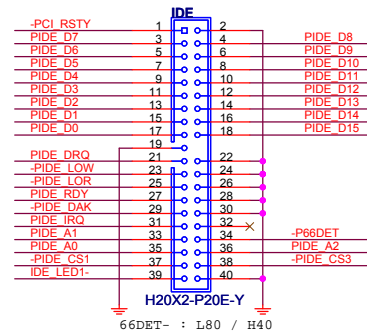
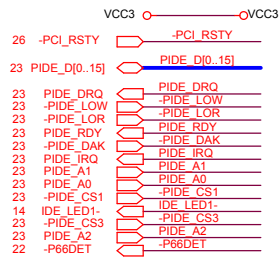
INT:E  
IDSEL:AD16



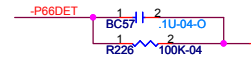
<b>Elitegroup Computer Systems</b>			
<b>PCI Slot, LPC DEBUG CARD</b>			
Title	Document Number	Rev	
Size	Custom	<b>A880GM-M6</b>	
Date: Thursday, April 29, 2010	Sheet 27 of 36	Rev 1.0	



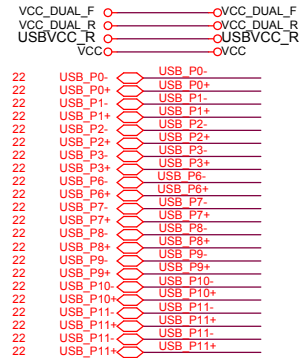
## External Connection



		ATI	Intel	NV	VIA	Sis
Pin 3	PDD7	X	Pull Hi: 4.7K	Pull Hi: 4.7K	Pull Hi: 4.7K	X
Pin 21	PDDRQ	X	Pull Hi: 8.2K	Pull Lo: 5.6K	Pull Hi: 4.7K	X
Pin 27	PIORDY	X	X	Pull Lo: 10K	Pull Lo: 10K	Pull Lo: 5.6K
Pin 31	PIDE_IRQ	X	X	Pull Lo: 5.6K	Pull Lo: 5.6K	X
Pin 34	P66DET-	100K	27K	15K	10K	20K

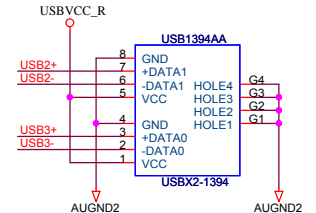
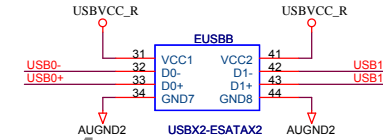
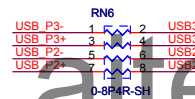
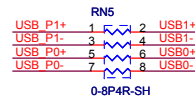
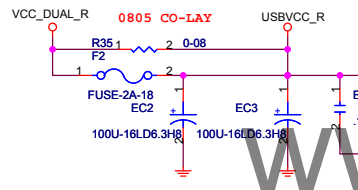


## External Connection

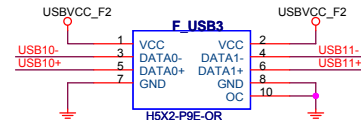
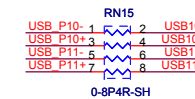
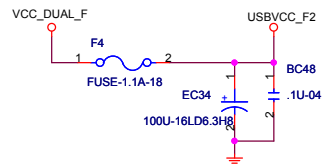
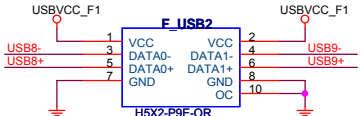
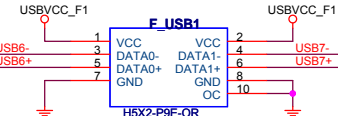
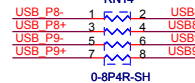
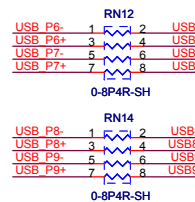
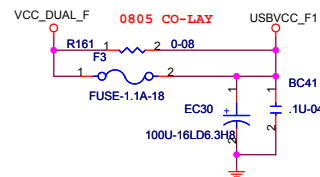


150 Mils Width

Power for Rear USB Ports



Power for Front USB Ports





VCC1.8

R87

0.08

DVDD\_18

1 2

1 2

0.1u-10VX-04

0.1u-10VX-04

JPERX+

JPERX-

Output

Change to Input

16 GPP\_RX2P

16 GPP\_RX2N

16 GPP\_TX2P

16 GPP\_TX2N

10 ESATA\_CLKP

10 ESATA\_CLKN

26,30 -PCI\_RSTX

14 ESATA\_LED-

CK\_PE\_100M\_SATA\_H

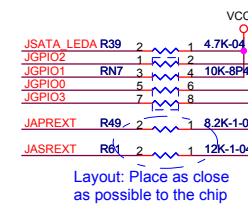
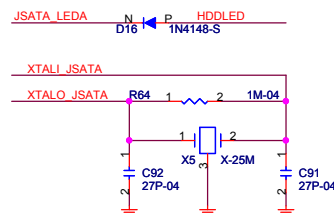
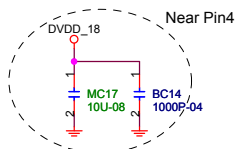
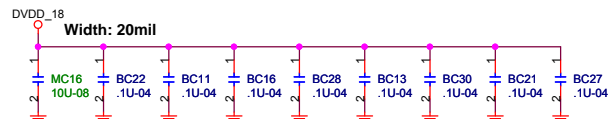
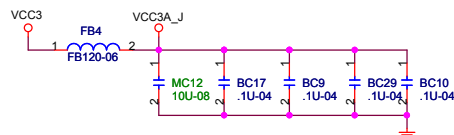
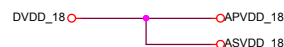
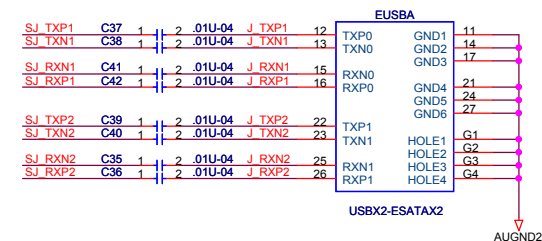
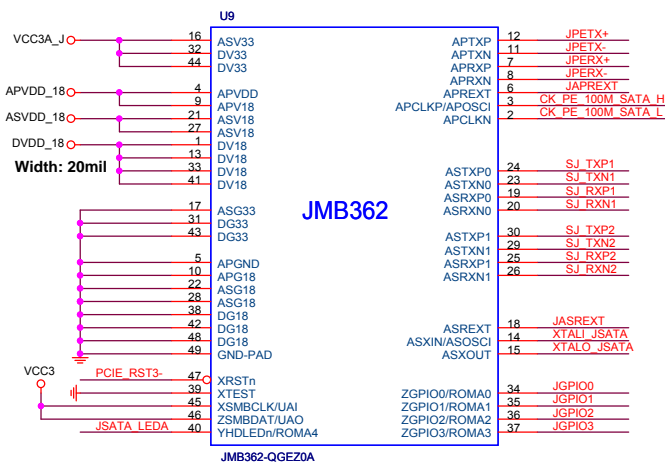
CK\_PE\_100M\_SATA\_L

PCIE\_RST3-

HDDLED

Chang to X7R 09/06/08

### Input

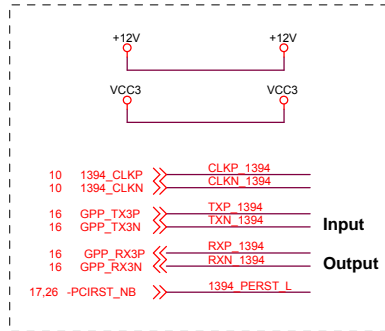






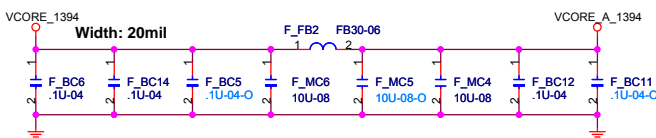
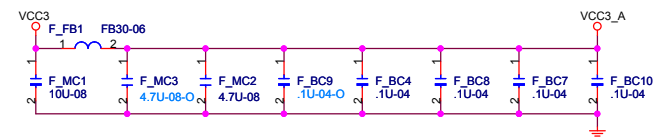
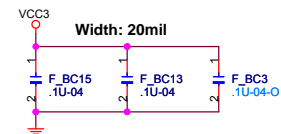


## External Connection

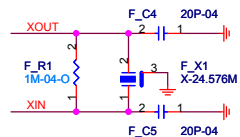


Trace Impedance=110 ohm +/- 6 ohm, L< 6"  
Differential Length Mismatch L<5mil

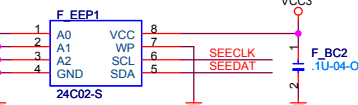
shadow EEPROM	ON	OFF
EE_EN	V	X



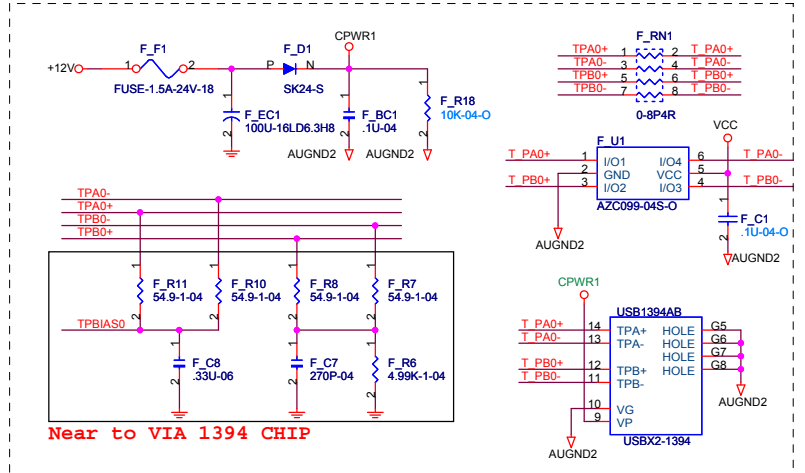
PCle Differential pair= 100 OHM



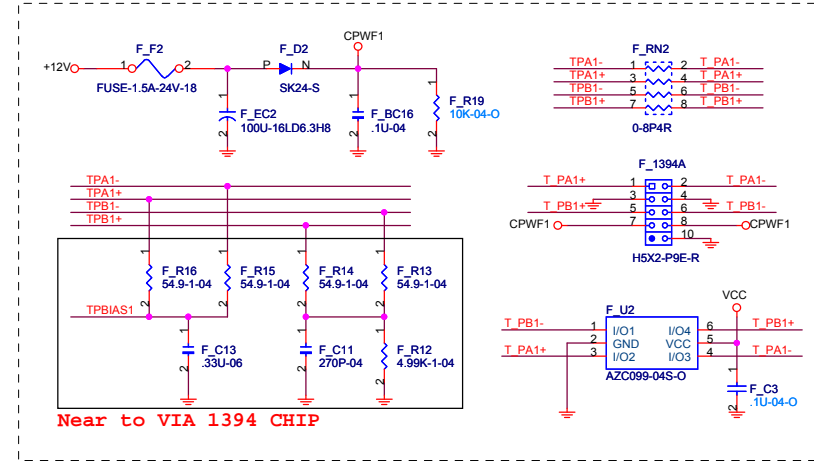
Xout, Xin (W:S)5:15mil  
close to chips



## Rear I/O

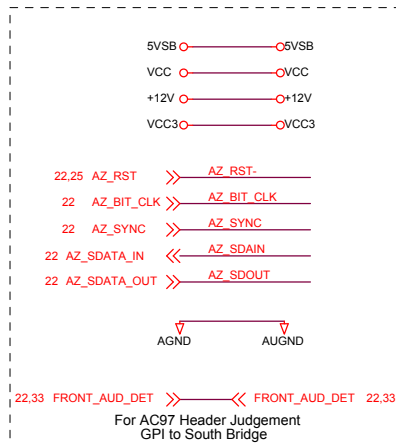


## Front 1394 Panel

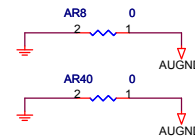




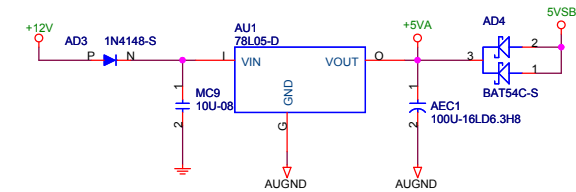
## External Connection



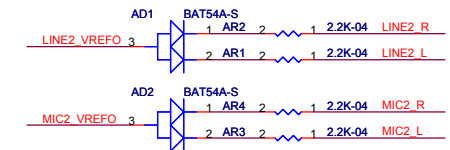
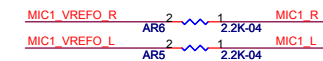
When you found some bug, please inform Ren(ext:665) to update circuit.



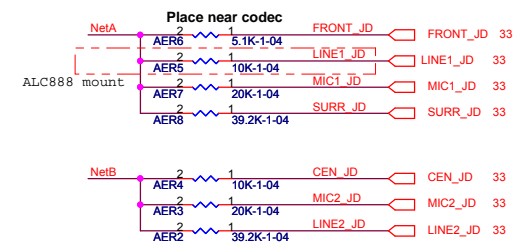
Improve the background noise of MIC boost



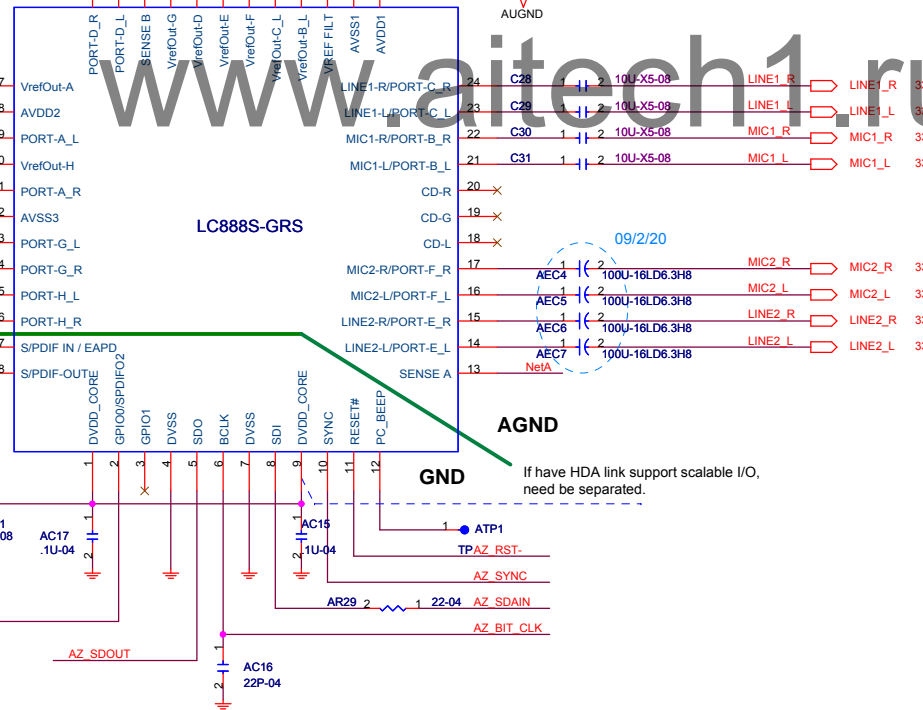
Verfourt bias for stereo microphone.



## Resistors Networks



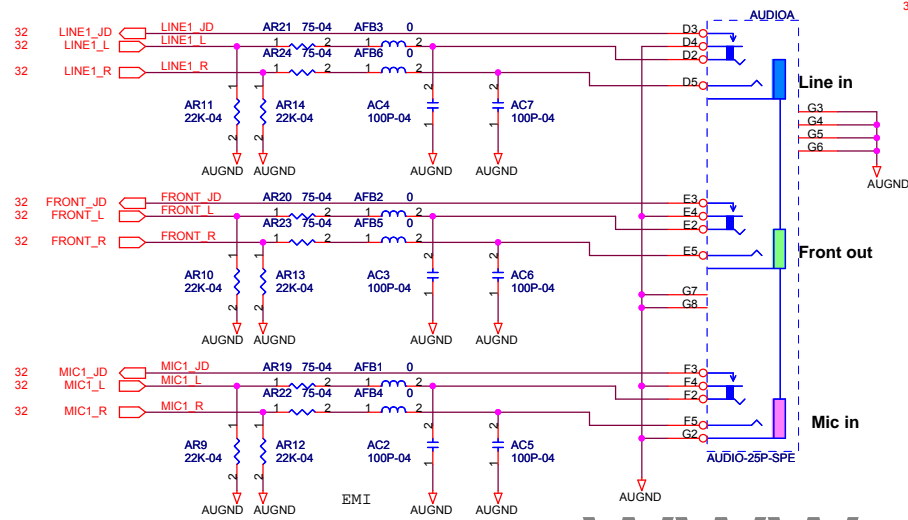
## CODEC



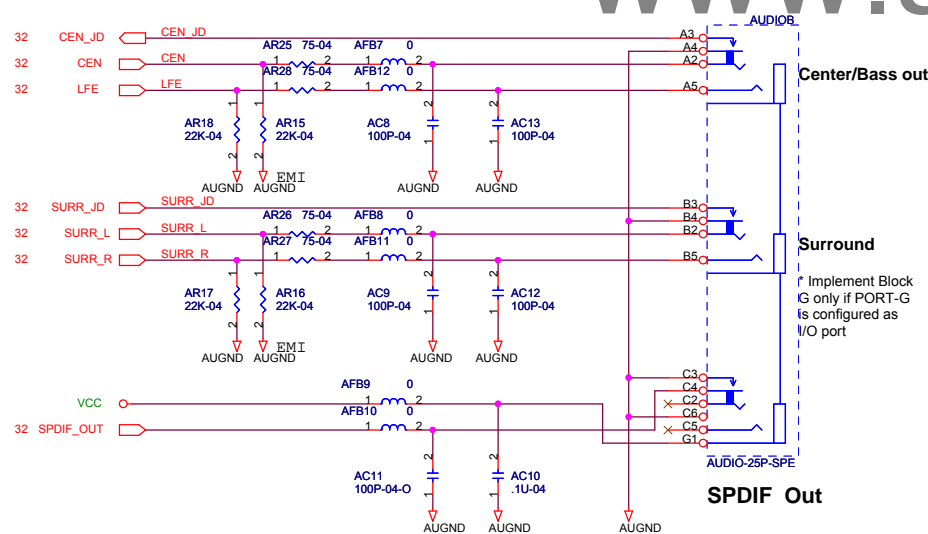


08.05.08 follow Realtek's suggestion

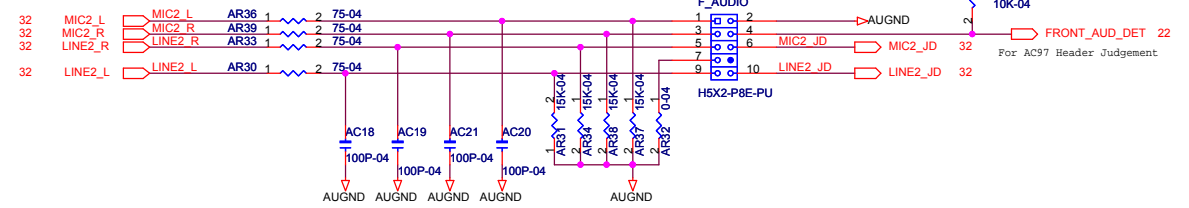
# Rear Panel Onboard Analog I/O



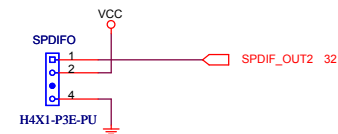
## Rear Panel (Optional Rear Audio Panel)



Follow Realtek's suggestion

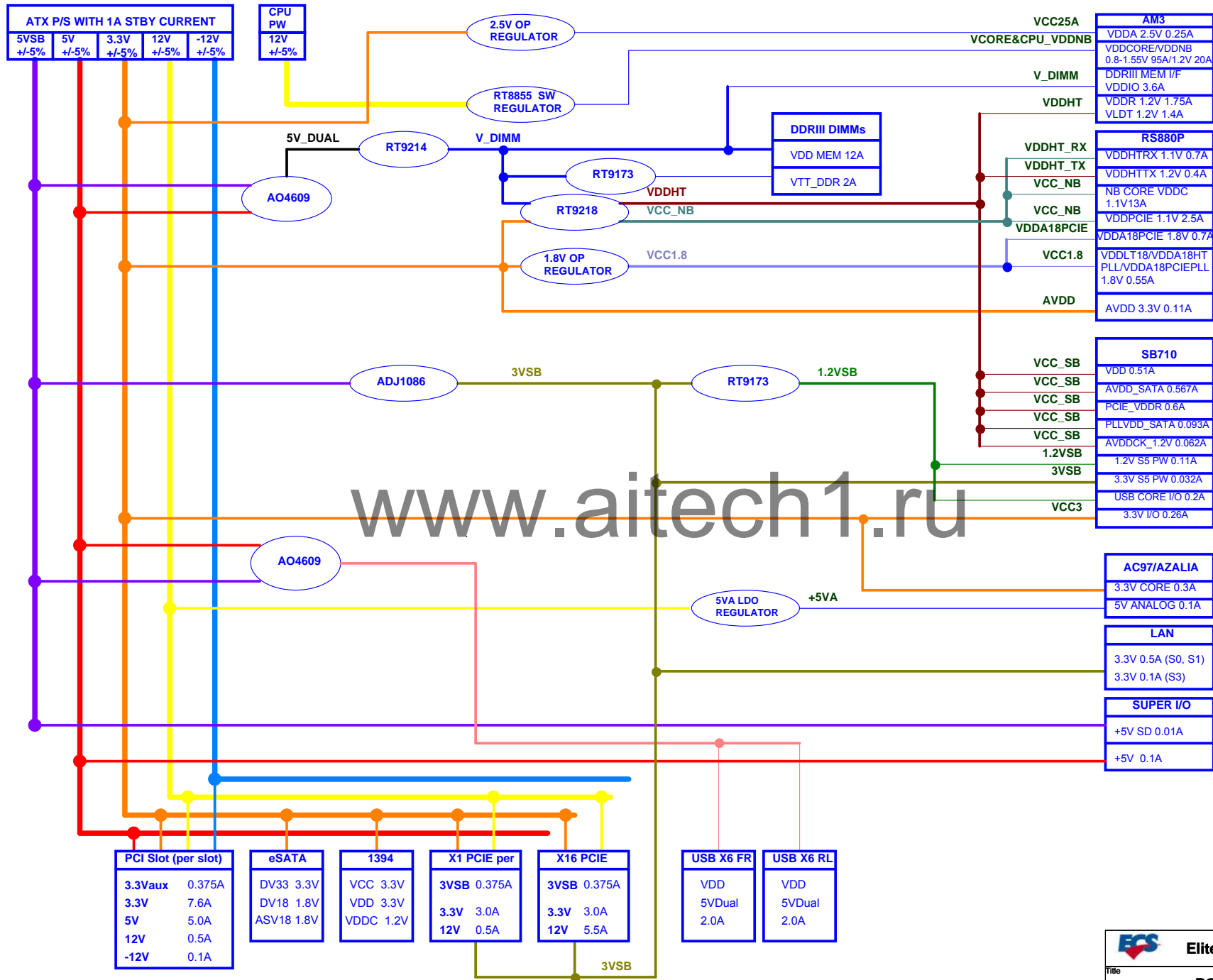


## SPDIF Out

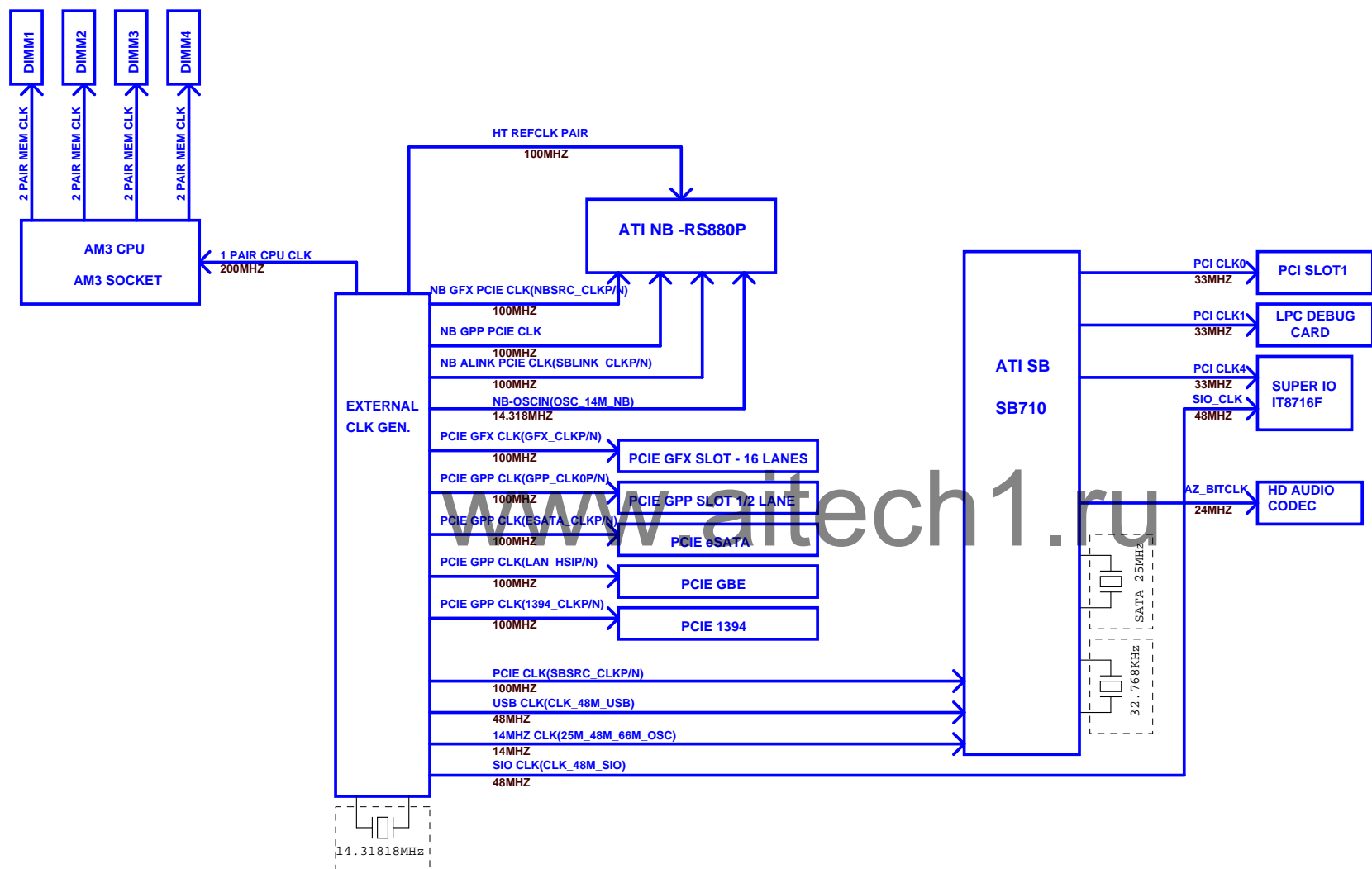


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# Power Sequence

